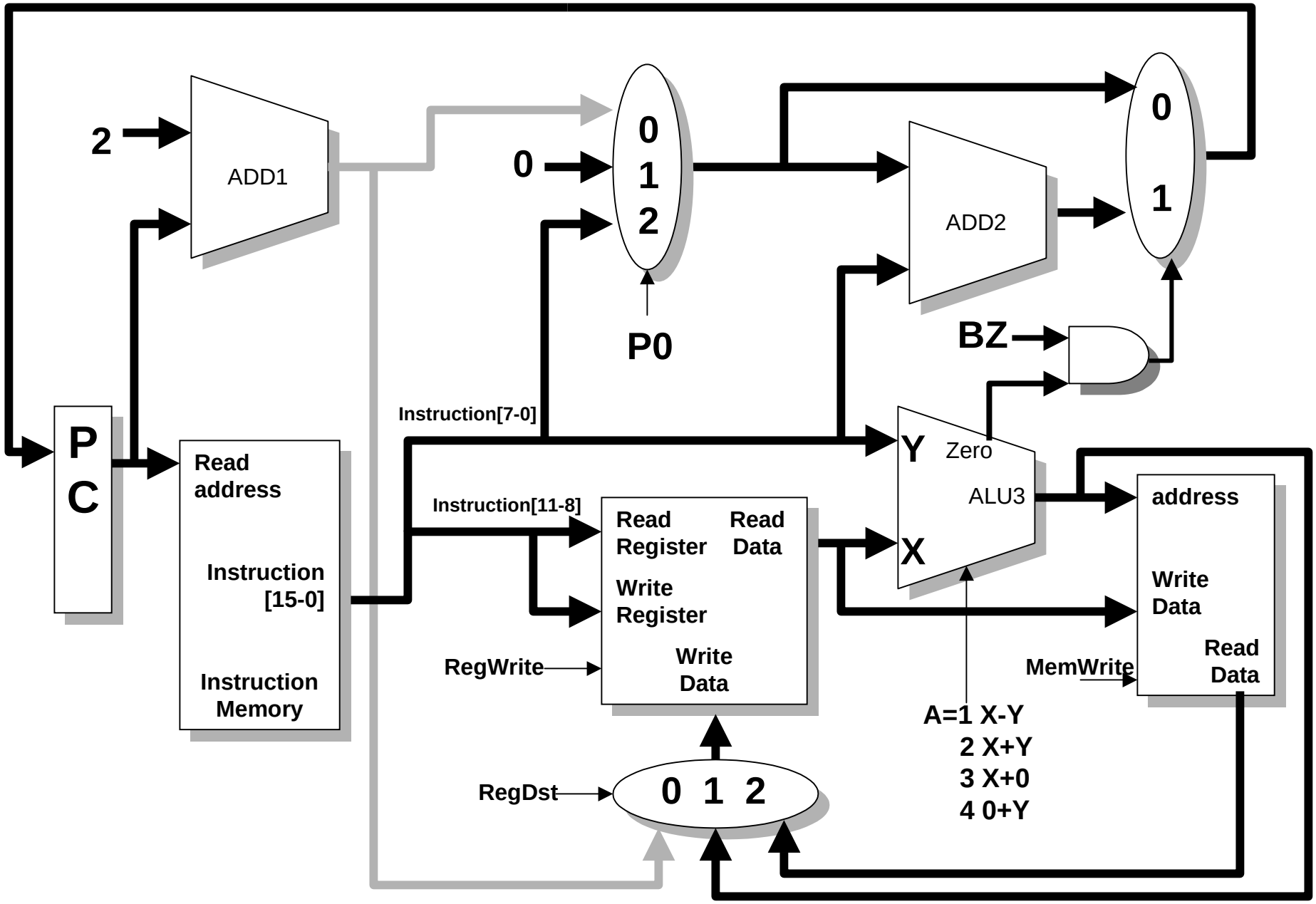
EECS 322 Test 3 Solutions Wednesday March 22, 2000

Problem 1 (50%): A group of EECS students have decided to compete with Intel Corporation in the microcontroller market. Their first prototype called the RISCEE1 computer is a 16 bit single-cycle computer build in a secret lab in Olin building.
The all 16 registers, pc, and alu are eight bits wide. Register zero (r0) contains only a zero and cannot be overwritten. There is only one instruction format shown as follows:

Opcode 4 bits 15-12	Register 4 bits 11-8	Data or Address field 8 bits 7-0

The delay time of the functional units are as follows Memory Write 5 ns, Memory Read 3 ns, Register (read or write) 2 ns, and ALU & Adders 2 ns.

RISCEE 1 Architecture



(a, 10%) Fill in the settings of the control lines determined by the all the instructions (use X for Don't Care)

Instruction	Operation	RegDst	A	MemWrite	RegWrite	BZ	P0
addi reg, data8	reg = reg + data8	1	2	0	1	0	0
subi reg, data8	reg = reg - data8	1	1	0	1	0	0
load reg, address8	reg = Memory[address8]	2	4	0	1	0	0
store reg, address8	Memory[address8]=reg	X	4	1	0	0	0
beq reg, address8	if(reg==0) {pc=pc+2+address8}	X	3	0	0	1	0
jmp address8	pc=address8	X	X	0	0	0	2
jal reg, address8	reg=pc+2; pc=address8	0	X	0	1	0	2

(b, 10%) Write "fail" for instructions that will stuck-at-fault for RegDst

Instruction	Stuck-at-0	Stuck-at-1
addi reg, data8	fail	
subi reg, data8	fail	
load reg, address8	fail	fail
store reg, address8		
beq reg, address8		
jmp address8		
jal reg, address8		fail

(c, 10%) Fill in the critical path times for each instruction

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles
addi	3 ns	2 ns	2 ns		2 ns	9 ns	1
subi	3 ns	2 ns	2 ns		2 ns	9 ns	1
load	3 ns		2 ns	3 ns	2 ns	10 ns	1
store	3 ns	2 ns	2 ns	5 ns		12 ns	1
beq	3 ns	2 ns	2 ns			7 ns	1
jmp	3 ns					3 ns	1
jal	3 ns				2 ns	5 ns	1

(d, 10%) Fill in the Clock, CPI, and MIPS in the above table and show all calculations (Hint, single-cycle computer).

Clock speed	83.3 Mhz	= 1/12ns=83.3 Mhs Clock speed is the slowest instruction
CPI	1	= 1*0.40+1*0.0+1*0.25+1*0.10+1*0.25+1*0+1*0
MIPS	83.3 MIPS	= 83.3 Mhz/1

(e, 10%) Using the RISCEE1 instruction set, show how to swap two registers r1 and r2 (hint, use memory).

Pick any 2 memory addresses, say, 100 and 102

```
store   r1, 100
store   r2, 102
load    r1,102
load    r2,100
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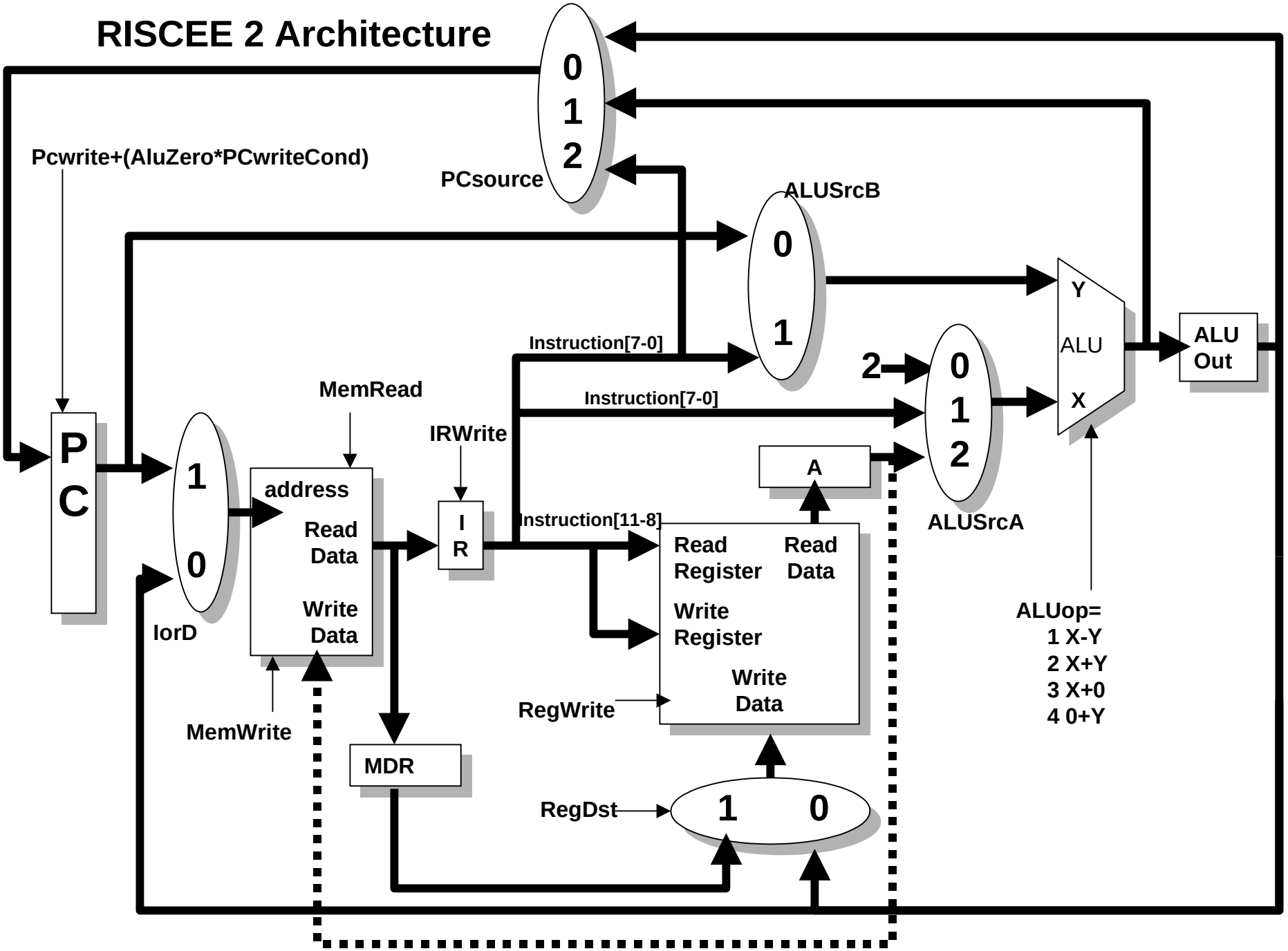
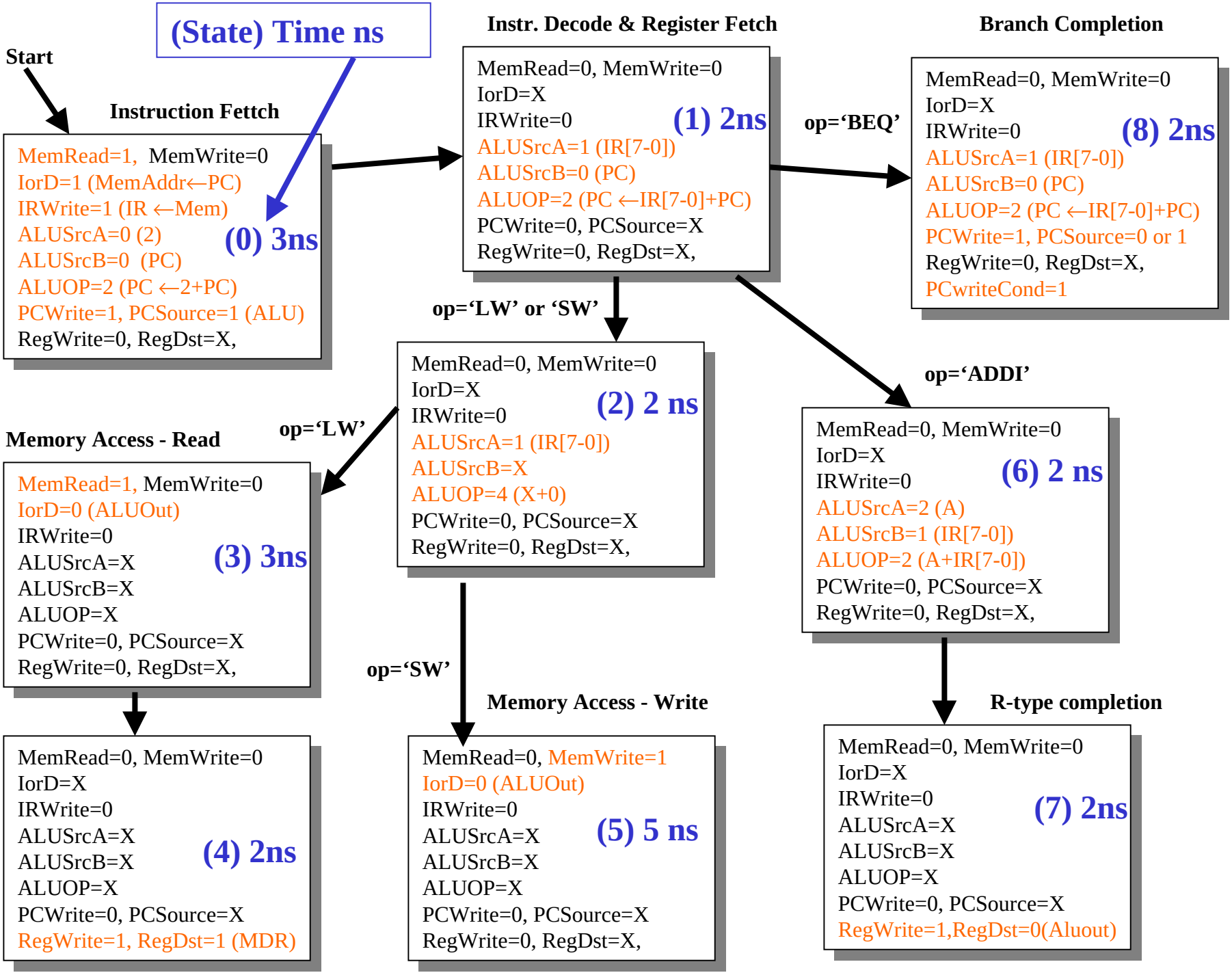
Problem 2 (50%): The brokerage firm said they talked to their investors and said they will only invest in multi-cycle computers . Furthermore, CPU Benchmarks showed that the subi, jmp, and jal instructions are not used. The multi-cycle version is called RISCEE 2.

(a, 20%) Draw the finite state machine for RISCEE instructions (addi, load, store, beq).

(b, 5%)Place next to each state the amount of to process each state.

see next page


RISCEE 2 Architecture
0
1
2
Pcwrite+(AluZero*PCwriteCond)
PCsource
ALUSrcB
0
1
Y
ALU
X
ALU
Out
Instruction[7-0]
2
0
1
2
Instruction[7-0]
MemRead
IRWrite
P
C
1
0
address
Read
Data
Write
Data
I
R
Instruction[11-8]
A
ALUSrcA
Read
Register
Read
Data
Write
Register
Write
Data
IorD
MemWrite
RegWrite
MDR
RegDst
1
0
ALUop=
1 X-Y
2 X+Y
3 X+0
4 0+Y


(State) Time ns
Start
Instruction Fettch
MemRead=1, MemWrite=0
IorD=1 (MemAddr←PC)
IRWrite=1 (IR ←Mem)
ALUSrcA=0 (2)
ALUSrcB=0 (PC)
ALUOP=2 (PC ←2+PC)
PCWrite=1, PCSource=1 (ALU)
RegWrite=0, RegDst=X,
(0) 3ns
Instr. Decode & Register Fetch
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=1 (IR[7-0])
ALUSrcB=0 (PC)
ALUOP=2 (PC ←IR[7-0]+PC)
PCWrite=0, PCSource=X
RegWrite=0, RegDst=X,
(1) 2ns
op='BEQ'
Branch Completion
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=1 (IR[7-0])
ALUSrcB=0 (PC)
ALUOP=2 (PC ←IR[7-0]+PC)
PCWrite=1, PCSource=0 or 1
RegWrite=0, RegDst=X,
PCwriteCond=1
(8) 2ns
op='LW' or 'SW'
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=1 (IR[7-0])
ALUSrcB=X
ALUOP=4 (X+0)
PCWrite=0, PCSource=X
RegWrite=0, RegDst=X,
(2) 2 ns
op='ADDI'
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=2 (A)
ALUSrcB=1 (IR[7-0])
ALUOP=2 (A+IR[7-0])
PCWrite=0, PCSource=X
RegWrite=0, RegDst=X,
(6) 2 ns
op='LW'
Memory Access - Read
MemRead=1, MemWrite=0
IorD=0 (ALUOut)
IRWrite=0
ALUSrcA=X
ALUSrcB=X
ALUOP=X
PCWrite=0, PCSource=X
RegWrite=0, RegDst=X,
(3) 3ns
op='SW'
Memory Access - Write
MemRead=0, MemWrite=1
IorD=0 (ALUOut)
IRWrite=0
ALUSrcA=X
ALUSrcB=X
ALUOP=X
PCWrite=0, PCSource=X
RegWrite=0, RegDst=X,
(5) 5 ns
R-type completion
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=X
ALUSrcB=X
ALUOP=X
PCWrite=0, PCSource=X
RegWrite=1,RegDst=0(Aluout)
(7) 2ns
MemRead=0, MemWrite=0
IorD=X
IRWrite=0
ALUSrcA=X
ALUSrcB=X
ALUOP=X
PCWrite=0, PCSource=X
RegWrite=1, RegDst=1 (MDR)
(4) 2ns

2 (c, 5%) Fill in critical path times for each instruction (copy delay times from part b).

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles
addi	3 ns	2 ns	2 ns		2 ns	9 ns	4
load	3 ns	2 ns	2 ns	3 ns	2 ns	12 ns	5
store	3 ns	2 ns	2 ns	5 ns		12 ns	4
beq	3 ns	2 ns	2 ns			7 ns	3

2 (d, 5%) Determine the fastest clock speed for the computer to work properly in frequency and show why.

Clock period is the slowest resource in any one step: 5 ns

Clock frequency = 1/period = 1/5ns = 200 Mhz

2 (d, 10%) Fill in the Clock, CPI, and MIPS in the above table and show all calculations.

Instruction	Clock Cycles	Instruction Mix
addi	4	40%
load	5	25%
store	4	10%
beq	3	25%
Clock speed	200 Mhz	
CPI	4	= 4*0.40+5*0.25+4*0.10+3*0.25
MIPS	50 MIPS	= 200 Mhz/4

2 (f, 5%) Suppose you do not know the instruction mix. Explain which one functional unit (Memory write 5ns, Memory Read 3ns, Register 2ns, ALU 2ns) would you chose to improve by 1 ns and what will be the new clock speed? (show calculations)

The clock period is determined by the slowest resource at any one stage,which is in this case the memory write speed of 5ns.

Therefor improving the memory write from 5ns to 4ns will change the

clock speed from 1/5ns (=200Mhz) to 1/4ns (=250Mhz).