Name: _____

Problem 1 (15%). Given the following "spatial" **direct-mapped** cache with 2 word blocks:
All instructions use byte addresses. The address bus is 10 bits. A word size is 16 bits.
Each cache entry (i.e. block size) contains 2 words. Total data cache size 16 words.

1a. (5%) How many bits is the index?

1b. (2%) How many bits is the byte offset?

1c. (1%) How many bits is the tag size?

1d. (7%) For the following instruction sequence, fill in the access bits to the **data cache**

tag	index	byte offset	instruction
			lw $1, 16($0)
			sw $3, 24($0)
			lui $1, 12
			lbu $5, 15($0)
			sltiu $1, $2, 32

Problem 2 (15%). Given the following **4-way set associative** cache architecture:
All instructions use byte addresses. The address bus is 10 bits. A word size is 32 bits.
Total data cache size 16 words.

2a. (5%) How many bits is the index?

2b. (2%) How many bits is the byte offset?

2c. (1%) How many bits is the tag size?

2d. (2%) For the following instruction sequence, fill in the access bits to the **data cache**

tag	index	byte offset	instruction
			lw $1, 12($0)
			lbu $2, 13($0)

2f. (5%) Increase the cache block size from 1 word to 2. How many bits is in the index?

Problem 3. (15%) For the following instruction sequence fill in the direct-mapped cache
The word size is 16 bits.
Memory[0]=0x1066; Memory[8]=0x1453; Memory[16]=$3=0x1776; Memory[24]=0x1914;

3a. (5%) Fill in the miss cache column.

tag	index	byte offset	instruction	Valid or Tag Cache Miss?
000	00	0	lw $1, 0($0)	
011	00	0	lw $2, 24($0)	
010	00	0	sw $3, 16($0)	
010	00	1	lbu $5, 17($0)	
001	00	0	lw $6, 8($0)	

3b. (10%) Show **all states** and **underline the final state** of the direct mapped data cache:

index	valid	tag	data
00			
01			
10			
11			

Problem 4. (15%) For the following instruction sequence fill in the 2-way set associative LRU cache
The word size is 16 bits.
Memory[0]=0x1066; Memory[8]=0x1453; Memory[16]=$3=0x1776; Memory[24]=0x1914;

4a. (5%) Fill in the miss cache column.

tag	index	byte offset	instruction	Valid or tag Cache Miss?
0000	0	0	lw $1, 0($0)	
0110	0	0	lw $2, 24($0)	
0100	0	0	sw $3, 16($0)	
0100	0	1	lbu $5, 17($0)	
0010	0	0	lw $6, 8($0)	

4b. (10%) Show **all states** and **underline the final state** of the 2-way set associative LRU data cache is:

index	valid	tag	data
0			
1			

Problem 5. (10%) Given a **two**-word cache entry block size and **one**-word wide memory bus organization (figure 7.13a, page 561), and the following access times:

2 clock cycle to send the address,
8 clock cycles to read access DRAM, 16 clock cycles to write to DRAM
3 clock cycle to to send a word

5a. (5%) What is the miss penalty for a write-through direct mapped cache?

5b. (5%) What is the miss penalty for a write-back direct mapped cache?

Problem 6 (20%). Given the following **virtual memory** architecture:

All instructions use byte addresses. The virtual address bus is 20 bits. A word is 16 bits.
Total page size 16 bytes. The real memory address bus is 16 bits.

6a. (4%) How many bits is the page offset?

6b. (4%) How many bits is the physical page number size?

6c. (4%) How many page table entries?

6d. (4%) How large is the page table?

6e. (4%) For the following instruction sequence, fill in the data access bits to the **page table**

virtual page number	page offset	instruction
		sw $1, 16($0)
		lw $2, 32($0)
		lbu $5, 33($0)

Problem 7. (10%) Assume 2048 bytes of real memory, LRU, a page size of 1024 bytes and no pages loaded in memory. Fill in the page fault columns. (Blank space implies No)

instruction	Page fault?	Flush which page?	Write flushed page to disk?	Load what new page
lw $1, 0($0)				
lw $2, 1024($0)				
lbu $5, 0($0)				
sw $6, 2048($0)				
lw $7, 1024($0)				
lw $1, 0($0)				
lw $2, 1032($0)				