1(a) (5 points) Fill in the truth table for the following logic and assume zero gate delay.

1(b) (20 points) Now fill in the timing diagram where each time step is 1 nanosecond and include the triggering lines using following gate delays: AND is 1 nanosecond delay, OR has 1 nanosecond delay and the NAND gate has 2 ns delay.

1(c) (10 points) Redraw the logic diagram of problem 1 using only 2-input NOR gates. Do not use NANDs, NOTs, ANDS, ORs, XORs, XNORs, etc.
2(a) (15 points) Fill in the following function table of the CMOS circuit below and label all the CMOS drains (D) and sources (S) on the circuit. For the CMOS circuit, assume \( V_{dd} = 1 \) Volt and a \( V_t \), threshold voltage of zero. (note: possible outputs 0, 1, X=short, Z=no connection, U=unknown).

<table>
<thead>
<tr>
<th>Inputs</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>f</th>
</tr>
</thead>
<tbody>
<tr>
<td>b</td>
<td>c</td>
<td>( V_b )</td>
<td>( V_a )</td>
<td>on/off</td>
<td>( V_a )</td>
</tr>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>0</td>
<td>Z</td>
<td>off</td>
<td>Z</td>
</tr>
<tr>
<td>0 1</td>
<td>0 0</td>
<td>0</td>
<td>Z</td>
<td>off</td>
<td>Z</td>
</tr>
<tr>
<td>1 0</td>
<td>0 0</td>
<td>0</td>
<td>Z</td>
<td>off</td>
<td>Z</td>
</tr>
<tr>
<td>1 1</td>
<td>0 0</td>
<td>0</td>
<td>Z</td>
<td>off</td>
<td>Z</td>
</tr>
</tbody>
</table>

2(b) (20 points) Fill in the missing SPICE parameters below for the above CMOS circuit, Using a rise and fall time of 0.2 nanoseconds and the input signals from timing diagram of problem 1.

```
* M1 3 1 5 0 T1 W=3.6U L=1.2U
* M2 5 2 2 0 T1 W=3.6U L=1.2U
* M3 6 2 4 4 W1 W=3.6U L=1.2U
* M4 3 1 6 4 W1 W=3.6U L=1.2U
* + 4 0 DC=1.0
* Vdd 1 0 PWL\n* \n* Vb 2 0 PWL\n* \n* .TRAN 0.1N 9N\n* .MODEL T1 NMOS LEVEL=1 KP=48E-6 LAMBDA=0.032 VTO=0.88 GAMMA=0.66 PHI=0.7
* .MODEL W1 PMOS LEVEL=1 KP=16E-6 LAMBDA=0.044 VTO=-0.85 GAMMA=0.69 PHI=0.7
* .END
```
3. (10 points) Fill in the timing diagram for the following circuit using 1 ns delay for the NAND gate.

Zero NAND with anything is logical one.

4. For the following circuit:

4(a) (5 points) Give the Boolean expression for

\[ f(a, b, c, d) = (a \cdot b) + (c \oplus d) \]

4(b) (5 points) Give the VHDL in one statement for

\[ f <= (a \text{ NAND} b) \text{ NOR} (c \text{ XOR} d) \]

4(c) (5 points) Give the C++/JAVA using "bitwise" operators in one statement for

\[ f = \sim (\sim (a \oplus b)) \| (c \wedge d) \]

4(d) (5 points) Give the C++/JAVA using only "logical" operators in one statement for

\[ f = \oplus (\oplus (a \& \& b)) \| (\ominus c \& \& d) \| (c \& \& d) \]

(X1) (Extra Credit, 5 points): Write the Boolean expression for a Coffee machine which outputs coffee (f) whenever 30 cents or more is deposited. The machine can only accept only one nickel, one dime and one quarter. Assume the variables, a is nickel deposited, b is a dime deposited, c is a quarter deposited.

\[ f = c + c b = c (a + b) \]

\[ f = b \cdot c + a \cdot c + a b c \]

\[ = c (b + c) + a b c \]