#4

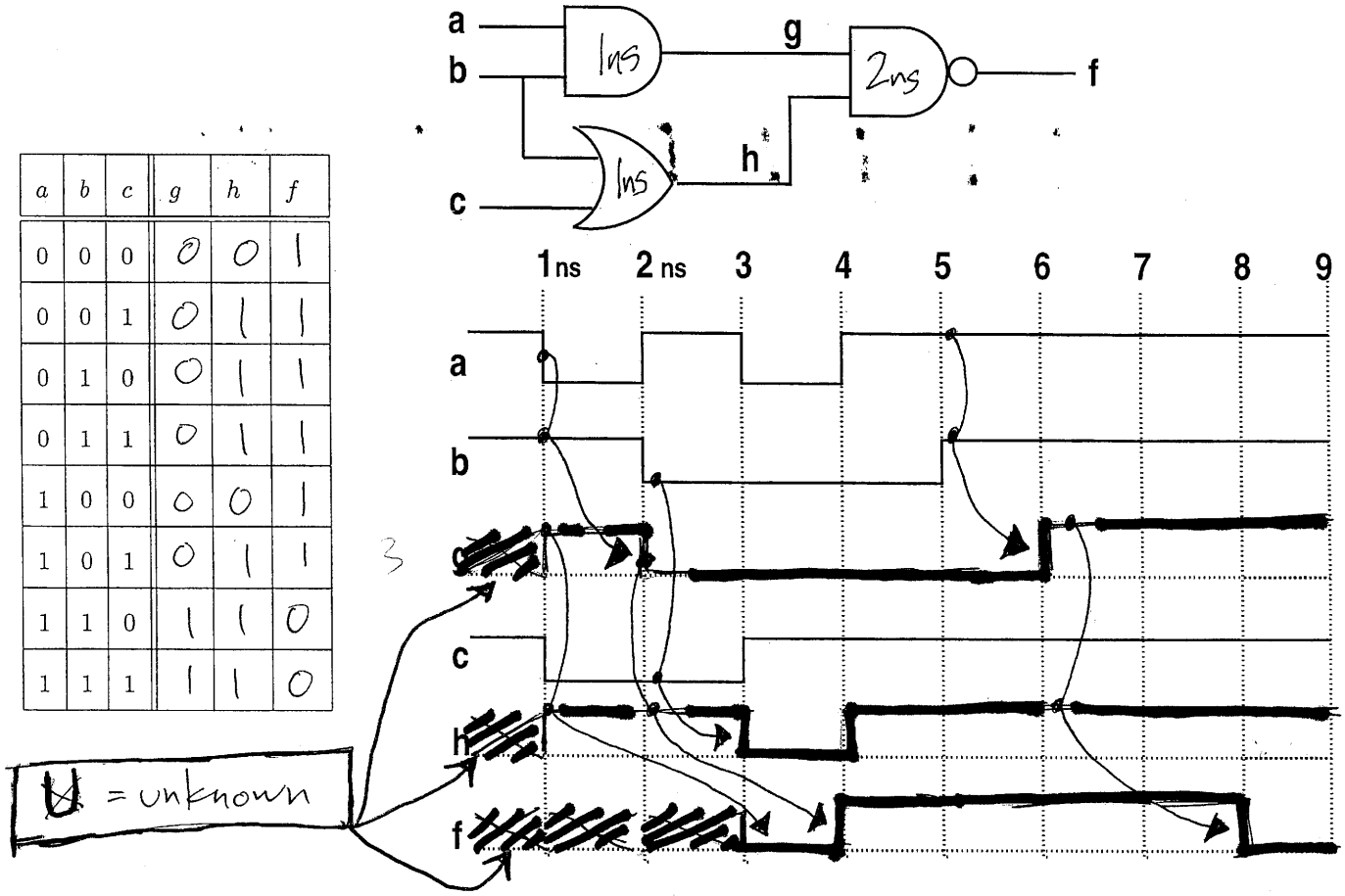
EECS 281: Solutions **Test 1 (3 pages)** **Due: Thursday, February 3, 2005**

Name: _____ Email: _____ Grade: _____ (100 max)

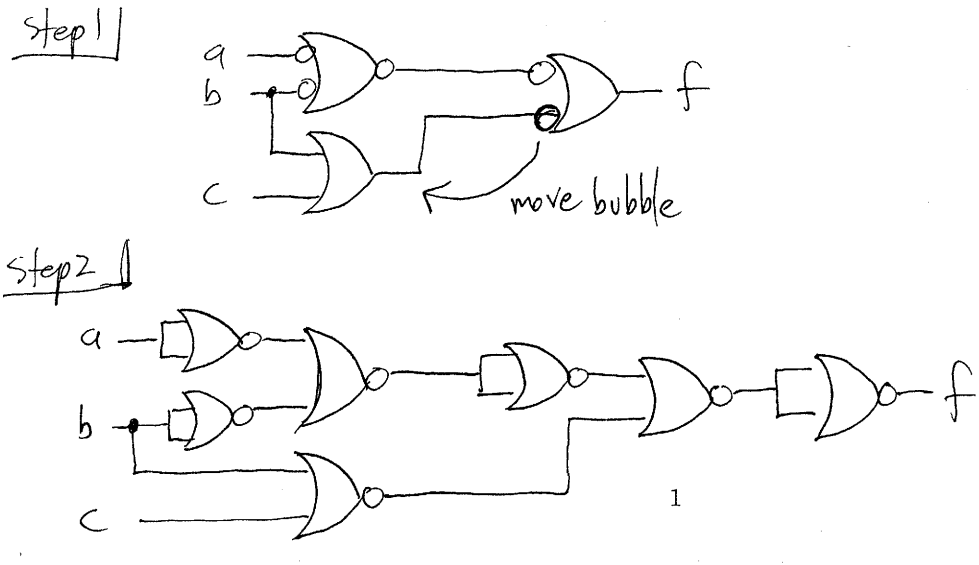
1(a) (5 points) Fill in the truth table for the following logic and assume zero gate delay.

1(b) (20 points) Now fill in the timing diagram where each time step is 1 nanosecond and include the **triggering lines** using following gate delays: AND is 1 nanosecond delay, OR has 1 nanosecond delay and the NAND gate has 2 ns delay.

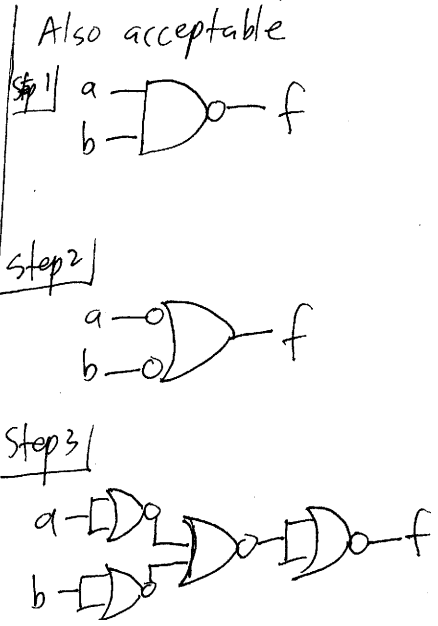
a	b	c	g	h	f
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	0	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	1	1	0



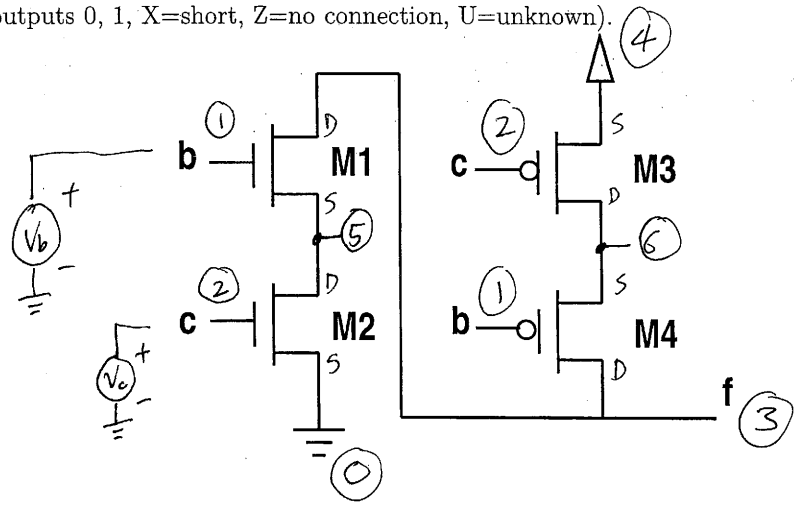
1(c) (10 points) Redraw the logic diagram of problem 1 using **only 2-input NOR gates**. Do not use NANDs, NOTs, ANDS, ORs, XORs, XNORs, etc.



Also acceptable



2(a) (15 points) Fill in the following function table of the CMOS circuit below and label all the CMOS drains (D) and sources (S) on the circuit. For the CMOS circuit, assume $V_{dd} = 1$ Volt and a V_t, threshold voltage of zero. (note: possible outputs 0, 1, X=short, Z=no connection, U=unknown).



-1 for every 4 errors

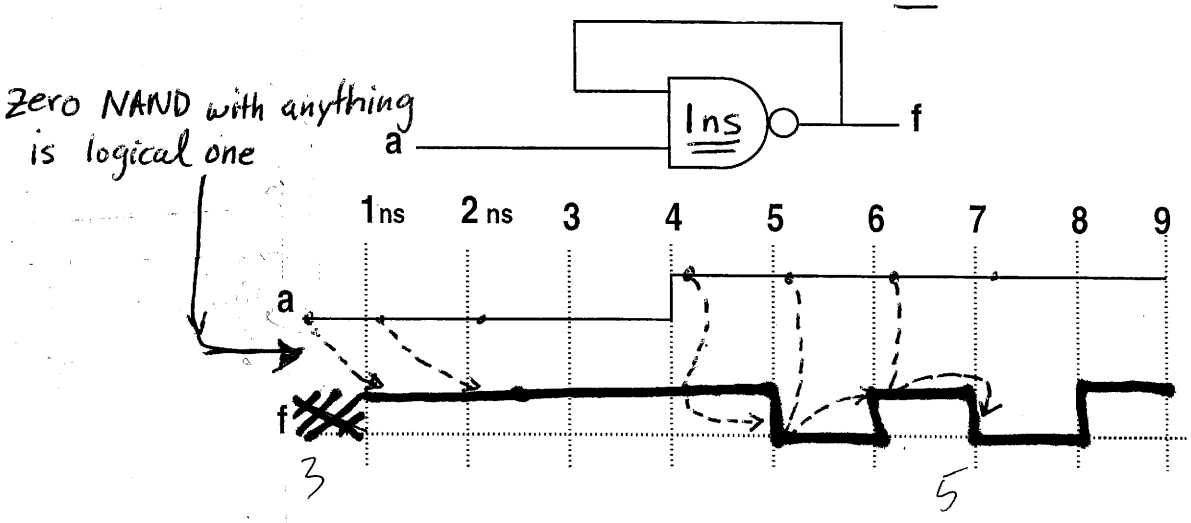
Inputs		M1				M2				M3				M4				f
b	c	V_g	V_s	on/off	V_d	V_g	V_s	on/off	V_d	V_g	V_s	on/off	V_d	V_g	V_s	on/off	V_d	f
0	0	0	Z	off	Z	0	0	off	Z	0	1	on	1	0	1	on	1	1
0	1	0	0	off	Z	1	0	on	0	1	1	off	Z	0	Z	off	Z	Z
1	0	1	Z	off	Z	0	0	off	Z	0	1	on	1	1	1	off	Z	Z
1	1	1	0	ON	0	1	0	on	0	1	1	off	Z	1	Z	off	Z	0

2(b) (20 points) Fill in the missing SPICE parameters below for the above CMOS circuit, Using a rise and fall time of 0.2 nanoseconds and the input signals from timing diagram of problem 1.

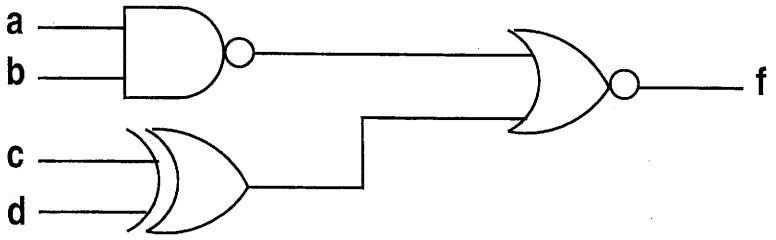
-1 for every 2 errors

```
          D    G    Src  Sub
*
M1        3    1    5    0     T1    W=3.6U  L=1.2U
M2        5    2    0    0     T1    W=3.6U  L=1.2U
M3        6    2    4    4     W1    W=3.6U  L=1.2U
M4        3    1    6    4     W1    W=3.6U  L=1.2U
*
Vdd       4    0    DC=1.0
*
Vb        1    0    PWL(  0N 1   2N 1   2.2N 0   5N 0   5.2N 1   9N 1  )
*
Vc        2    0    PWL(  0N 1   1N 1   1.2N 0   3N 0   3.2N 1   9N 1  )
*
.TRAN  0.1N   9N
*
.MODEL T1 NMOS LEVEL=1 KP=48E-6 LAMBDA=0.032 VTO=0.88  GAMMA=0.66 PHI=0.7

.MODEL W1 PMOS LEVEL=1 KP=16E-6 LAMBDA=0.044 VTO=-0.85 GAMMA=0.69 PHI=0.7

.END
```

3. (10 points) Fill in the timing diagram for the following circuit using 1 ns delay for the NAND gate.



4 For the following circuit:



4(a) (5 points) Give the Boolean expression for

$f(a,b,c,d) =$ $\overline{(a \cdot b)} + (c \oplus d)$

4(b) (5 points) Give the VHDL in one statement for

f <= (a NAND b) NOR (C XOR D)

4(c) (5 points) Give the C++/JAVA using "bitwise" operators in one statement for

f = ~(~(a & b)) | (c ^ d)

4(d) (5 points) Give the C++/JAVA using **only** "logical" operators in one statement for

f = !(!(a && b)) || ((!c && d) || (c && !d))

(X1) (Extra Credit, 5 points): Write the Boolean expression for a Coffee machine which outputs coffee (f) whenever 30 cents or more is deposited. The machine can only accept only one nickel, one dime and one quarter. Assume the variables, a is nickel deposited, b is a dime deposited, c is a quarter deposited.

$f = ca + cb = c(a+b)$ $\quad f = b \cdot c + a \cdot c + abc$

$= c(b+c) + abc$