1. Given the following schematic (study Wakerly p410-p413)

(a) Give the Truth Table for $a$, $b$, $w$, $u$ and $f$.

<table>
<thead>
<tr>
<th>$a$</th>
<th>$b$</th>
<th>$x$</th>
<th>$w$</th>
<th>$u$</th>
<th>$f$</th>
</tr>
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<tbody>
<tr>
<td>0</td>
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(b) Give the structural boolean expression of $w$, $u$ and $f$:

\[ w = a \oplus 1 \]
\[ u = a \oplus w = a \oplus (a \oplus 1) \]
\[ f(a, b) = u \oplus x = (a \oplus (a \oplus 1)) \oplus (b \oplus 0) \]

(c) Re-write as a structural VHDL expression:

\[ f \leftarrow (a \text{ XOR} (a \text{ XOR} 1)) \text{ XOR} (b \text{ XOR} 0) \]

(d) Re-write as a structural C++/JAVA expression using bitwise operators:

\[ f = (a \wedge (a \wedge 1)) \wedge (b \wedge 0) \]

(e) Looking at the Truth Table, what is the simplest Boolean expression

\[ f(a, b) = \overline{b} \]
2. Given the following logic circuits with inputs a, b and c (study Wakerly page 126, 385-387)

(a) Give the truth table for $f_1$ and $f_2$ showing $g$, $h$, $k$ and $m$. Calculate the outputs $g$ and $h$ as if they were not connected together in $f_1$. Calculate $f_1$ as with $g$ and $h$ connected as a single wire.

<table>
<thead>
<tr>
<th>c</th>
<th>a</th>
<th>b</th>
<th>upper gate</th>
<th>lower gate</th>
<th>g</th>
<th>h</th>
<th>f_1</th>
<th>k = c \cdot a</th>
<th>m = \overline{c} \cdot b</th>
<th>f_2 = k + m</th>
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<tbody>
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<td>dis</td>
<td>en</td>
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</table>

(b) Are $f_1$ and $f_2$ functionally (behaviourally) the same? Yes or No.
Are $f_1$ and $f_2$ structurally the same? Yes or No.
3. Give the timing diagram showing trigger lines for the following logic circuit (study Wakerly page 535) \textbf{Every gate 1 nanosecond delay}

Every gate 1 nanosecond delay
4. Do the following Wakerly problems (Due on Thursday)

(a) 3.14, page 185

Review

N MOS, n-channel, \( V_g - V_s > V_t \) is ON

PMOS, p-channel, \( V_g - V_s < V_t \) is ON

if \( V_t = 0 \) then

\( V_g > V_s \) or \( V_g > 0 \) is ON for NMOS

\( V_g < V_s \) or \( V_g < 0 \) is ON for PMOS

3.014

2 trans.

4 trans.

Inverter has fewer for CMOS technology.

In Figure 3-22, OAI page 95

let \( A = a \), \( B = 0 = \text{ground (Q4, Q3)} \), \( C = b \)

D = c

then replace Q4 with a wire from Drain to Source, remove Q3 the NMOS

attempt #1 = 8 transistors

a

b

a+a=a

a+0=0

b+c

attempt #2 = 6 transistors

because if we ground (=0) the input the we can replace the NMOS with open and the PMOS with a wire
In Figure 3-20, AOI-gate, page 94

Let $A = 1$ then

$A = 1$ means the NMOS at Q1 is always ON and the PMOS at Q2 is always OFF

So replace Q1 with a wire from drain to source remove Q2 the PMOS
\[ \overline{z} = a \overline{b} \]
\[ z = \overline{a b} \]

<table>
<thead>
<tr>
<th></th>
<th>a</th>
<th>b</th>
<th>( z )</th>
<th>( \overline{z} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \overline{a b} )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( \overline{a b} )</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( a \overline{b} )</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1 = a \overline{b} = \overline{z}</td>
</tr>
<tr>
<td>ab</td>
<td>1</td>
<td>1</td>
<td>1</td>
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\[ a \overline{b} \]
\[ b \]
\[ z \]
\[ 2T \]
\[ 4T \]