1. Given the following schematic (study Wakerly p410-p413)

(a) Give the Truth Table for \(a, b, w, u\) and \(f\).

(b) Give the structural boolean expression of \(w, u\) and \(f\):

\[ w = \]
\[ u = \]
\[ f(a, b) = \]

(c) Re-write as a structural VHDL expression:

\[ f <= \]

(d) Re-write as a structural C++/JAVA expression using bitwise operators:

\[ f = \]

(e) Looking at the Truth Table, what is the simplest Boolean expression

\[ f(a, b) = \]
2. Given the following logic circuits with inputs a, b and c (study Wakerly page 126, 385-387)

(a) Give the truth table for $f_1$ and $f_2$ showing $g$, $h$, $k$ and $m$. Calculate the outputs $g$ and $h$ as if they were not connected together in $f_1$. Calculate $f_1$ as with $g$ and $h$ connected as a single wire.

(b) Are $f_1$ and $f_2$ functionally (behaviourally) the same? Yes or No.
Are $f_1$ and $f_2$ structurally the same? Yes or No.
3. Give the timing diagram showing trigger lines for the following logic circuit (study Wakerly page 535)
4. Do the following Wakerly problems (Due on Thursday)

(a) 3.14, page 185
(a) 3.59, page 188
(a) 3.60, page 188
(a) 3.61, page 188
(a) 3.62, page 188