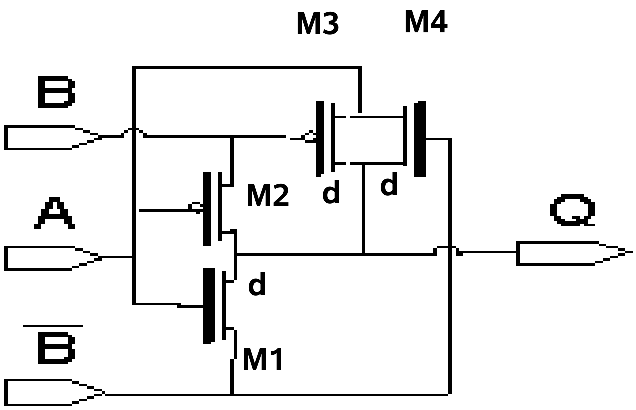
EECS 281 Sample Test 1 Due: Tuesday September 14, 2004
Name: ___________________________ Email:____________________________

(1) Determine the function table of the following circuit (note: all drains connect to Q):



		M1: nmos On=Vg>Vs				*M2: pmos On=Vg<Vs*				*M3: pmos On=Vg<Vs*				*M4: nmos on=Vg>Vs*				*Q*
		Vg	*Vs*	*on/off*	*Vd*	*Vg*	*Vs*	*on/off*	*Vd*	*Vg*	*Vs*	*on/off*	*Vd*	*Vg*	*Vs*	*on/off*	*Vd*	
A	**B**	**A**	**~B**			**A**	**B**			**B**	**A**			**~B**	**A**			
0	0	0	1	off	Z	0	0	off	Z	0	0	off	Z	1	0	on	0	0
0	1	0	0	off	Z	0	1	on	1	1	0	off	Z	0	0	off	Z	1
1	0	1	1	off	Z	1	0	off	Z	0	1	on	1	1	1	off	Z	1
1	1	1	0	on	0	1	1	off	Z	1	1	off	Z	0	1	off	Z	0

NMOS: if Vg>Vs then ON and Drain is connected to Source; else OFF;
PMOS: if Vg<Vs then ON and Drain is connected to Source; else OFF;

Q = M1(Vd) + M2(Vd) + M3(Vd) + M4(Vd);

(2) Write the SPICE .subchk for the circuit in problem 1.
(Given, A=1, B=2, BNOT=3, Q=4, VDD=5, PCH for PMOS, NCH for NMOS, W=5U, L=5U).

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.SUBCKT XOR1X   1 2 3 4 5
* .SUBCKT XOR1X A=1 B=2 BNOT=3 Q=4 VDD=5
*
*Mname DRAIN GATE SOURCE SUBSTRATE MODEL WIDTH   LENGTH
*      NODE  NODE NODE   NODE      NAME  MICRONS MICRONS
*----- ----- ---- ------ --------- ----  ------- ------
M1     4     1    3      0         NCH   W=5U    L=2U
M2     4     1    2      5         PCH   W=5U    L=2U
M3     4     2    1      5         PCH   W=5U    L=2U
M4     4     3    1      0         NCH   W=5U    L=2U
.ENDS XOR1X
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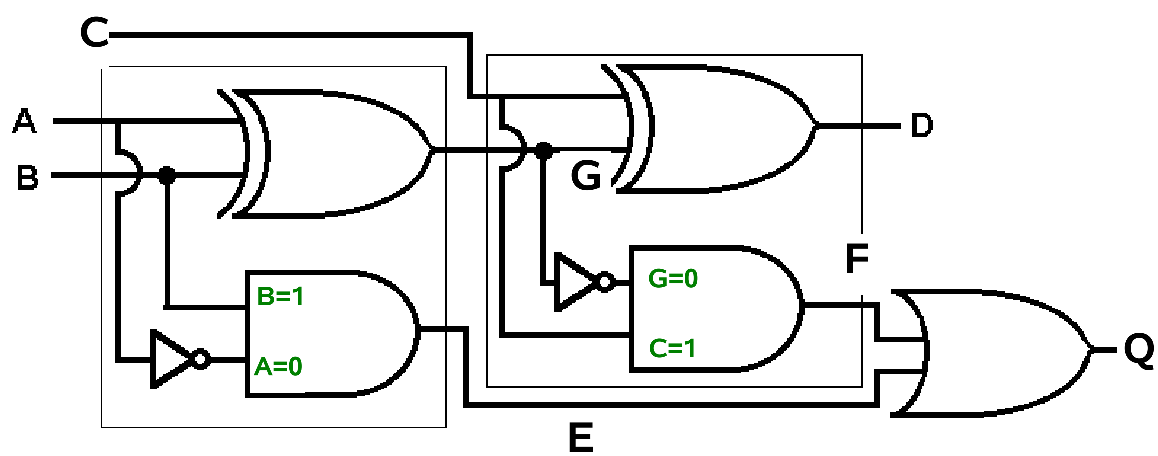
(3) Give the logical expression in VHDL notation for the following logic circuit:



D <= (C XOR (A XOR B));____

E <= NOT(A) AND B; F<=C AND NOT(G); G<=A XOR B; Q<=F OR E

Q <= (C AND NOT(A XOR B)) OR (NOT(A) AND B);________________________

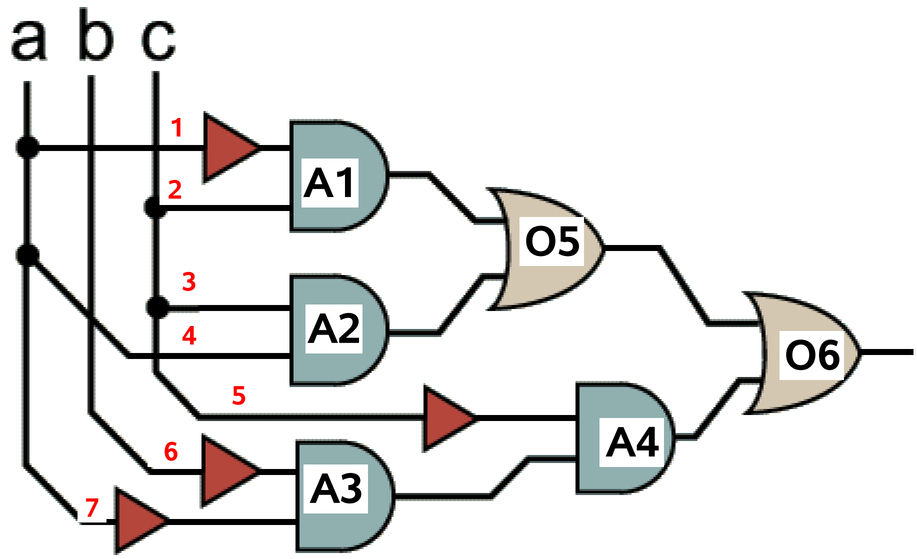
(4) Fill in the truth table: (blanks also mean false or zero).

For ANDs first fill in the trues (why only one case). For ORs fill in the falses first.
E = true only when A=0 and B=1;
G = true only when A or B is odd number of one bits.
F = true only when C=1 and G=0;
D=is it odd number of bits?;
Q = false only F=0 and E=0; then fill blanks with 1's;

A	*B*	*C*	*E*	*F*	*G*	*D*	*Q*
0	0	0					**0**
0	0	1		**1**		**1**	**1**
0	1	0	**1**		**1**	**1**	**1**
0	1	1	**1**		**1**		**1**
1	0	0			**1**	**1**	**0**
1	0	1			**1**		**0**
1	1	0					**0**
1	1	1		**1**		**1**	**1**

(5) Redraw problem 3 using only NOR Gates for output Q only.

(6) Given that NOT has delay of 10ns, NAND 20ns, and NOR 40ns for the following circuit what is the minimum and maximum delay and show work (note: circuit contains BUFFERs, ANDs, and ORs):



(a) Delay for a BUFFER is ___10ns+10ns = 20ns_________________
(b) Delay for AND using only NAND and NOT ___20ns+10ns=30ns________________
(c) Delay for OR using only NOR and NOT is ___40ns+10ns=50ns___________
(d) What is the minimum delay = 100ns______________ and through what gates: BUFFER+A4+O6_________
(e) What is the maximum delay = 150ns___________ and through what gates: BUFFER+A1+O5+O6___________

parh 1: (input a): BUFFER+A1+O5+O6 = 20 + 30 + 50 + 50 = 150 maximum
path 2: (input c): A1 + O5 + O6 = 30+50+50 = 130
path 3: (input c): A2 + O5 + O6 = 130
path 4: (input a): A2 + O5 + O6 = 130
path 5: (input c): BUFFER+A4+O6=20+30+50=100 minimum
path 6: (input b): BUFFER+A3+A4+O6=20+30+30+50=130
path 7: (input a): BUFFER+A3+A4+O6=130

(7) Design a logic expression for a coke machine which releases one coke can (Q) whenever the minimum amount of 20 cents is entered. The coin box outputs 3 signals when a 5 cent coin (A), 10 cent coin (B), and 25 cent coin (C) in parallel is received. The coin box will only accept at most one coin of each type. Please show work.

Q <= (NOT(A) AND NOT(B) AND C) OR (NOT(A) AND B AND C) OR (A AND NOT(B) AND C) OR (A AND B AND C);

A	*B*	*C*	*Total*	*Q*	*ANDs*
5¢	*10¢*	*25¢*			
0	0	0	**0¢**		
0	0	1	**25¢**	**1**	**~A & ~B & C**
0	1	0	**10¢**		
0	1	1	**35¢**	**1**	**~A & B & C**
1	0	0	**5¢**		
1	0	1	**30¢**	**1**	**A & ~B & C**
1	1	0	**15¢**		
1	1	1	**40¢**	**1**	**A & B & C**