Video Phone System Design

Brad Murray
Greg Lefty
Mike Halfen

ECES 488 Spring 2000

Introduction

Unique Design Features

- Button Scheme
- “Streamed Video”
- Time Stamp From Caller ID

User Defined System Constraints

- Require external power supply
- Plug directly to Telco Jack
- Maximum message length of 60 seconds
- Maximum of 30 messages
  - When message memory is filled, the oldest message is erased.
- Standalone device

Technical System Constraints

- Audio Sample Rate = 8K samples/second
- Audio Memory Requirement
  - 384 Kbyte/message
- QCIF Standard Video Format (176 x 144)
  - 304 Kbit/ frame
  - Compressed (20:1) = 15.2 Kbit/frame
  - At 1 frame/sec = 114 Kbyte/message
- Total Message Storage - 14.9 MB
- Additional DSP Data/Table Memory = 64K

Design Options

- Available Hardware Options
  - Off the shelf IC
  - DSP/Microcontroller
  - FPGA
  - ASIC
- Determining Factors
  - Design Cost
  - Production Cost
  - Flexibility

Component Comparison

Hardware Type	Design Cost	Production Cost	Flexibility
Shelf IC	None	Low	None
DSP/Micro Cont	Moderate	Low	High
FPGA	High	Low	Moderate
ASIC	Very High	Moderate	Low

The Competition

- Market segmented
  - Video calls over IP
    - Dominant segment
    - Extremely cheap ($70 for camera/software)
      - Hardware often consists only of digital camera
      - Software driven design
    - Computer, network connection required
  - Video over telephone
    - TV / Monitor products
      - Still cheap (< $300)
    - Display Integrated devices
      - Most Expensive

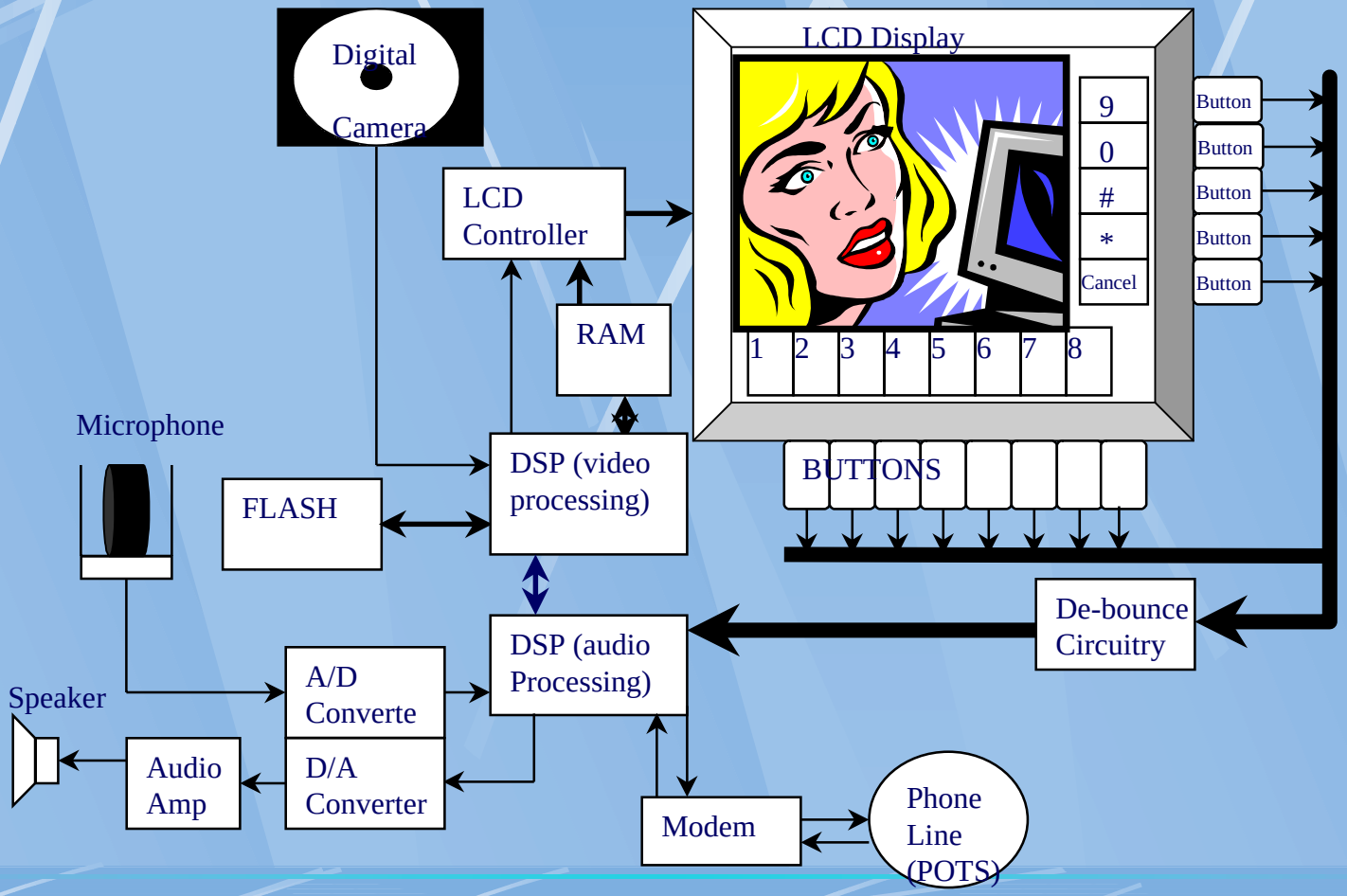
Display Integrated Videophones

- Common features
  - H.324 compliant
  - Able to send minimum of 7 frames/sec (up to 15!)
    - Use of QCIF standard (176 x 144 pixel picture transmitted)
  - Camera electronically adjustable: zoom, pan, tilt
  - 4” LCD Display: adjustable picture quality and size
  - Average retail price: $600
- Manufacturers
  - Aiptek
    - Cheap!! ~$450 at Amazon.com
    - Basic features only
  - MCF Enterprises (~$600)
    - Picture in Picture
    - Advanced standard telephone features
      - **Answering machine (voice only)**
      - **Redial & Number Memory**

Display Integrated Videophones

- Other Manufacturers
  - 8x8
    - Led market in this segment
    - Discontinued telephone products
      - Now manufactures H.323 products
        - Video conferencing over I.P.
      - Provides chip sets and development solutions for H.324
  - Panasonic
    - Only major electronics manufacturer in this market
    - Same features as Aiptek, 8x8
    - Priced 2 - 3 times higher ($1150!!)

System Overview



Components

- LCD Display
- Digital Camera
- Analog to Digital Converter (ADC)
- Digital to Analog Converter (DAC)
- Modem DSP
- Video DSP
- Memory

LCD Display

Requirements

- 320 x 240 resolution 8 bit color
- DSP Controlled
- Low Cost

Market Analysis

Vendor	PN	Price	Notes	Color/BW	Pixels/1000	Metric/Price
Hantronix	HDM3224-LC	$70.81	320x240 (Color)	30	77	$1.31
Epson	SED1335	$10.60	Controller for above LCD			
Newark Electronics	AND32222MST	$273.00	B/W 320x240	5	77	$0.30
Newark Electronics	AND711AST-30	$115.00	B/W (240x64)	5	15	$0.18
Lumex	LCM5240x128GSF	$78.00	240x128 B/W	5	31	$0.46
NEC	NL3224	$297.00	320x240 Color	30	77	$0.36
Sharp	LQ039Q2DS54	$250.00	320x240 Color	30	77	$0.43
Crystalloid	CR32240	$70.00	320x240 (B/W)	5	77	$1.17

Digital Camera

Requirements

- 320 x 240 resolution 8 bit color
- DSP Controlled
- Low Cost

Market Analysis

Vendor	PN	Price	Notes
Allied	CVC-50BC/PH	$89.00	Color Board
Stark Electronic	V-X0095-PCB-3.6	$79.00	Color Board - NTSC

ADC / DAC

Requirements

- 8,000 Samples per Second
- 8 bits per Sample
- Low Cost

Market Analysis

Vendor	PN	Price	Bits	Speed MHz
Fairchild	ADC0804	$2.00	8	10
Phillips	TDA8792M/C2	$6.40	8	25
National Semiconductor	ADC0804	$2.00	8	10
FSC/Raymill	ADC0804	$2.00	8	10

Vendor	PN	Price	Bits	Speed MHz
Fairchild	DAC0808LCMX	$1.37	8	6.67
Phillips	TDA8702TD-T	$1.84	8	30
National Semiconductor	DAC0808LCM	$0.81	8	6.67
FSC/Raymill	DAC0808	$1.37	8	6.67

Memory

Requirements

- Maintain 30 Messages
  - 60 Seconds each
- Communicate with Video DSP
- Large Flash Memory for Message Storage
- Small Memory for Program and Data Space
- Low Cost

Market Analysis

Vendor	PN	Price	Notes	Size Metric	Metric/Price
Bright (Winbond)	BM29F040	$6.50	4Mb Flash - 90ns sector erase	4.00	$0.62
Sharp	LH28F008SCTL85	$10.39	8 MB Flash - 64K block erase	8.00	$0.77
Sharp	LH28F004SCTL85	$8.78	4 MB Flash - 64K block erase	4.00	$0.46
Sharp	LH28F160SCBL95	$13.01	3V-FLASH 16 MEG - Block Erase	16.00	$1.23
Sharp	LH5164A	$2.07	64K SRAM - 8K*8 arrangement	0.06	$0.03

Audio DSP

Requirements

- Communicate with Video DSP
- Process Audio (ADC/DAC)
- Communicate with Modem
- H.324 Compliance
  - Mux/Demux modem data
    - H.223 Protocol
  - Process Inter-terminal communication
    - H.245 Protocol
- Low Cost

Video DSP

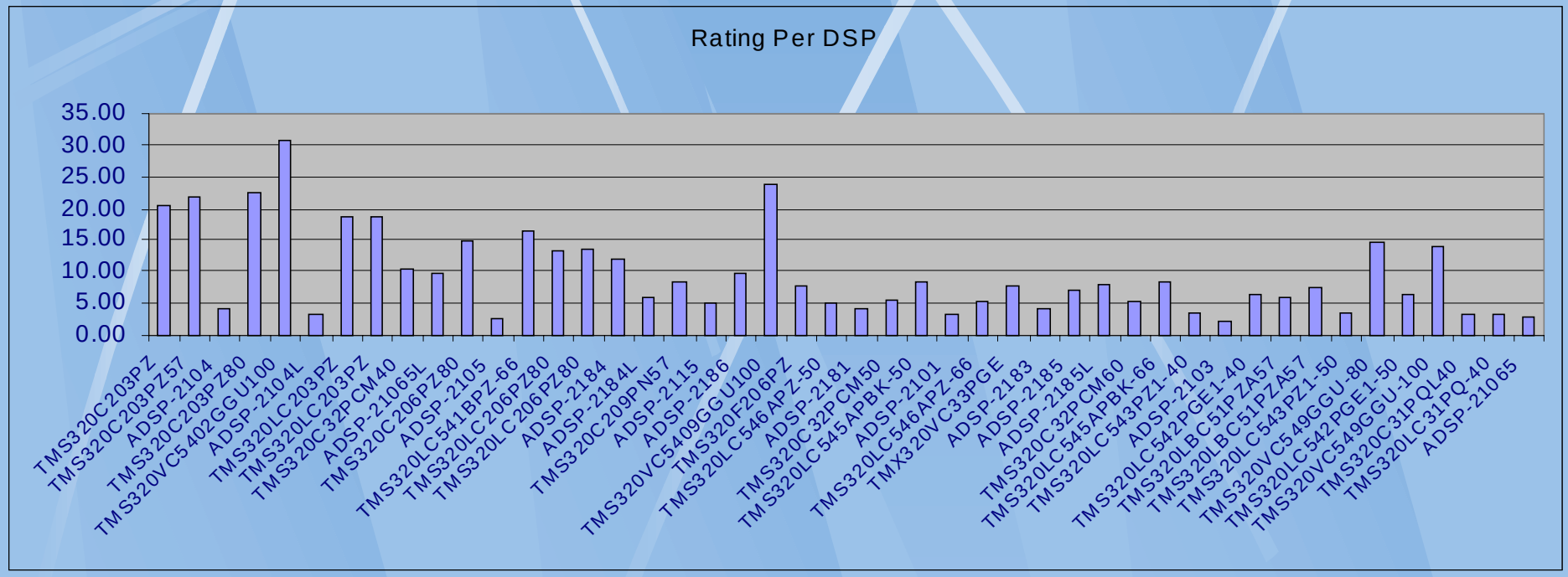
Requirements

- Communicate with Modem DSP
- Receive and Compress Camera Data
- Decompress and Send LCD Data
- Encode/Decode Video Data
  - H.263 Protocol for H.324 Compliance
- Store and Retrieve Messages

DSP Evaluation

- Speed
- # of Interfaces
  - Serial
  - Parallel
- Cost
- Bit capability
  - ALU
  - Bus width
  - Registers

DSP Market Analysis



TI TMS320VC35402

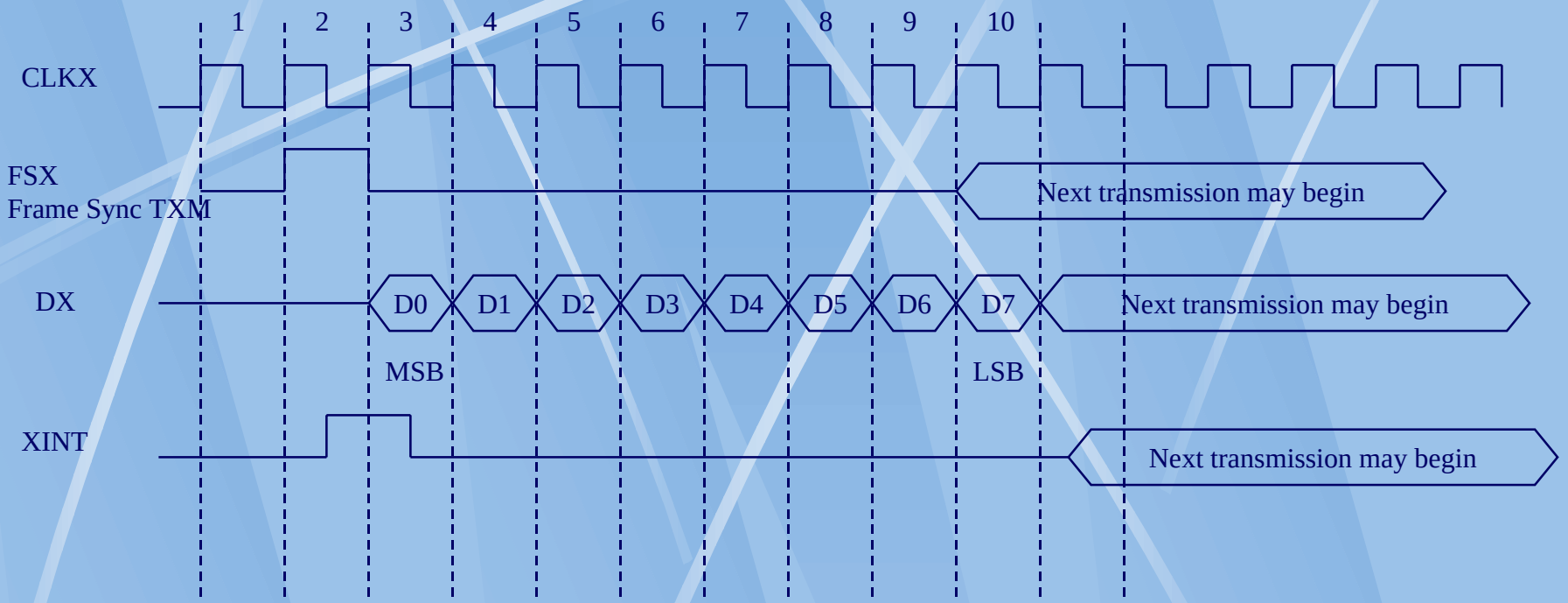
Pricing Analysis Summary

Handtronix	LCD Display	$70.81
Epson	LCD Controller	$10.60
Philips	Modem Interface	$8.00
Cermtek	Modem DAA	$16.67
Stark Electronic	Camera	$79.00
Sharp	Flash Memory	$13.01
Sharp	SRAM	$2.07
National Semiconductor	ADC	$2.00
National Semiconductor	DAC	$0.81
Texas Instruments	Audio DSP	$6.94
Texas Instruments	Video DSP	$6.94
Labor & Engineering (per unit)		$18
	Total Cost	**$234.85**

Bus Interfaces

- Serial Interface
  - Digital Camera
  - AD/DA converters
- HPI Interface
  - DSP – DSP communication
- Parallel
  - Memory
  - LCD Controller

Serial Port Interface: Transmitting



Clock 1: Data is loaded into output register

Clock 2, rising edge: Frame sync signal is generated

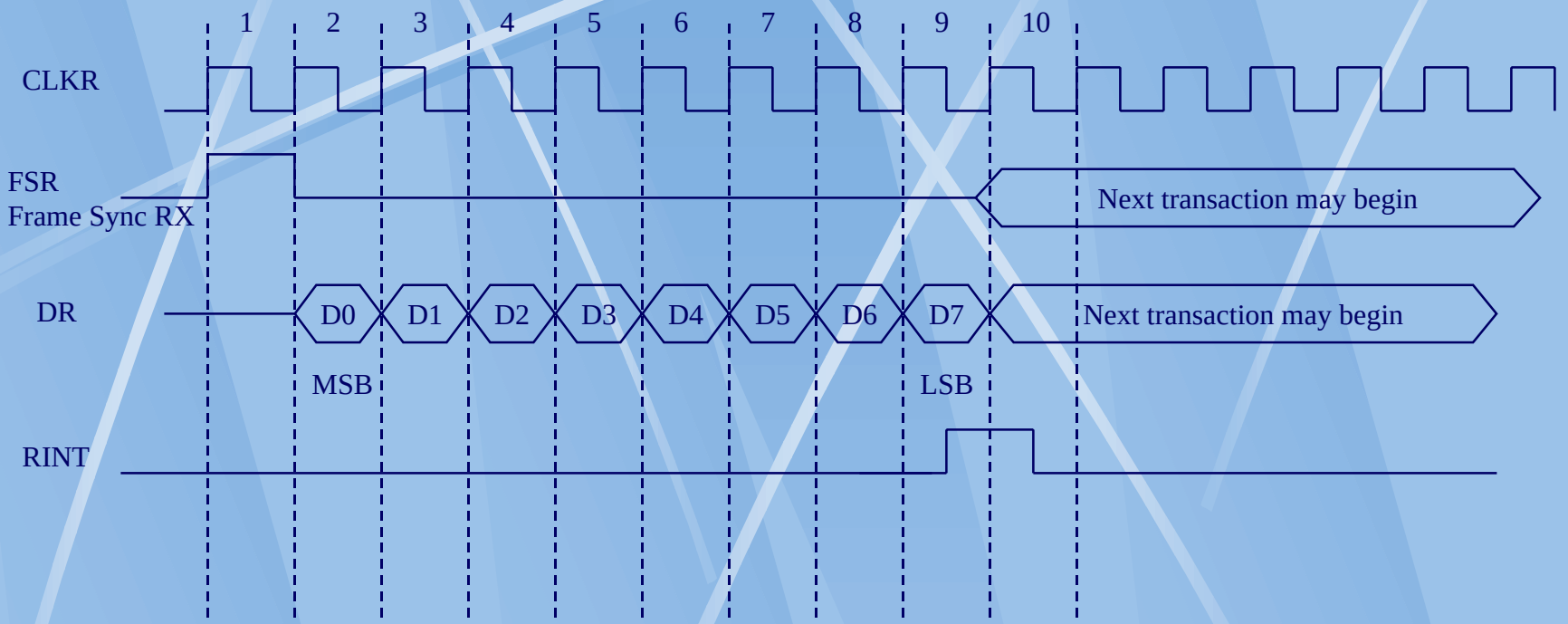
Clock 2, falling edge: Interrupt generated to indicate transmission has begun

Clock 3..10: One data bit is sent on each rising clock edge

Clock 9: New data may be loaded into output register

Clock 10: If output register was loaded, frame sync signal is generated

Serial Port Interface: Receiving



Clock 1: Frame sync is generated

Clock 2..9: One data bit is sampled on each falling clock edge

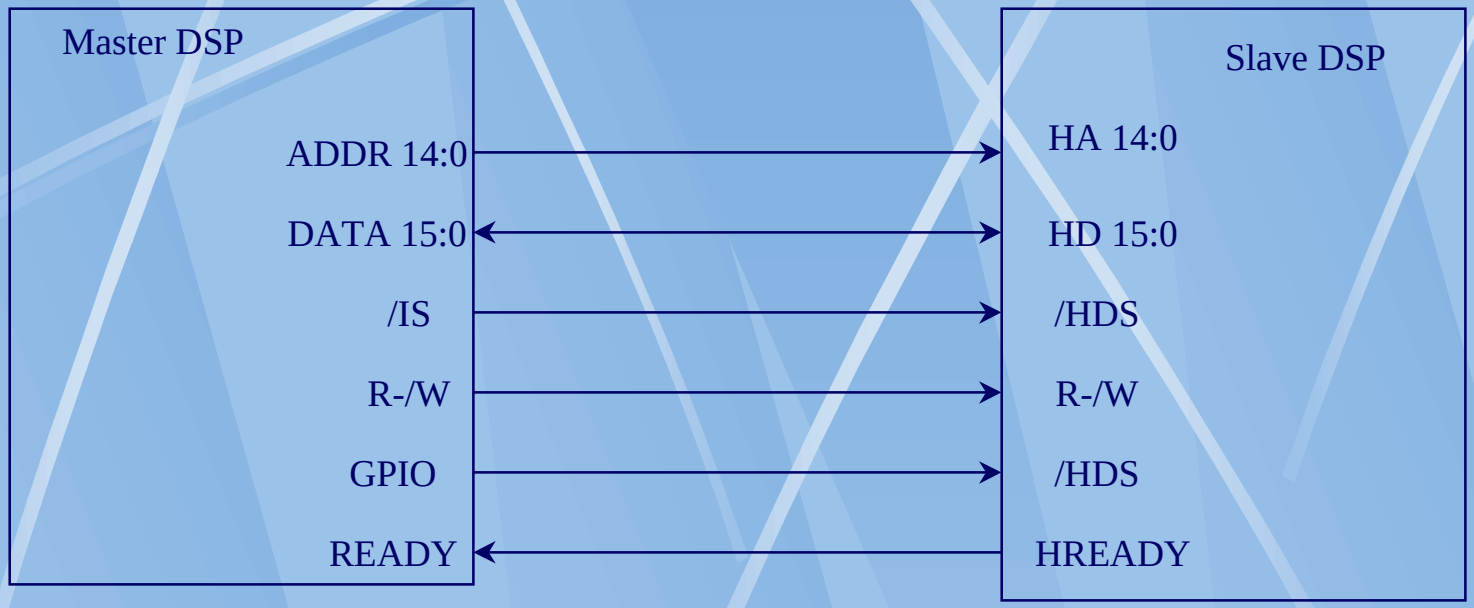
Clock 9, falling edge: Interrupt generated to indicate data is ready in receive register

Clock 10, rising edge: Frame sync may be generated for next transaction

Clock 10: If frame sync generated, MSB of next byte is received

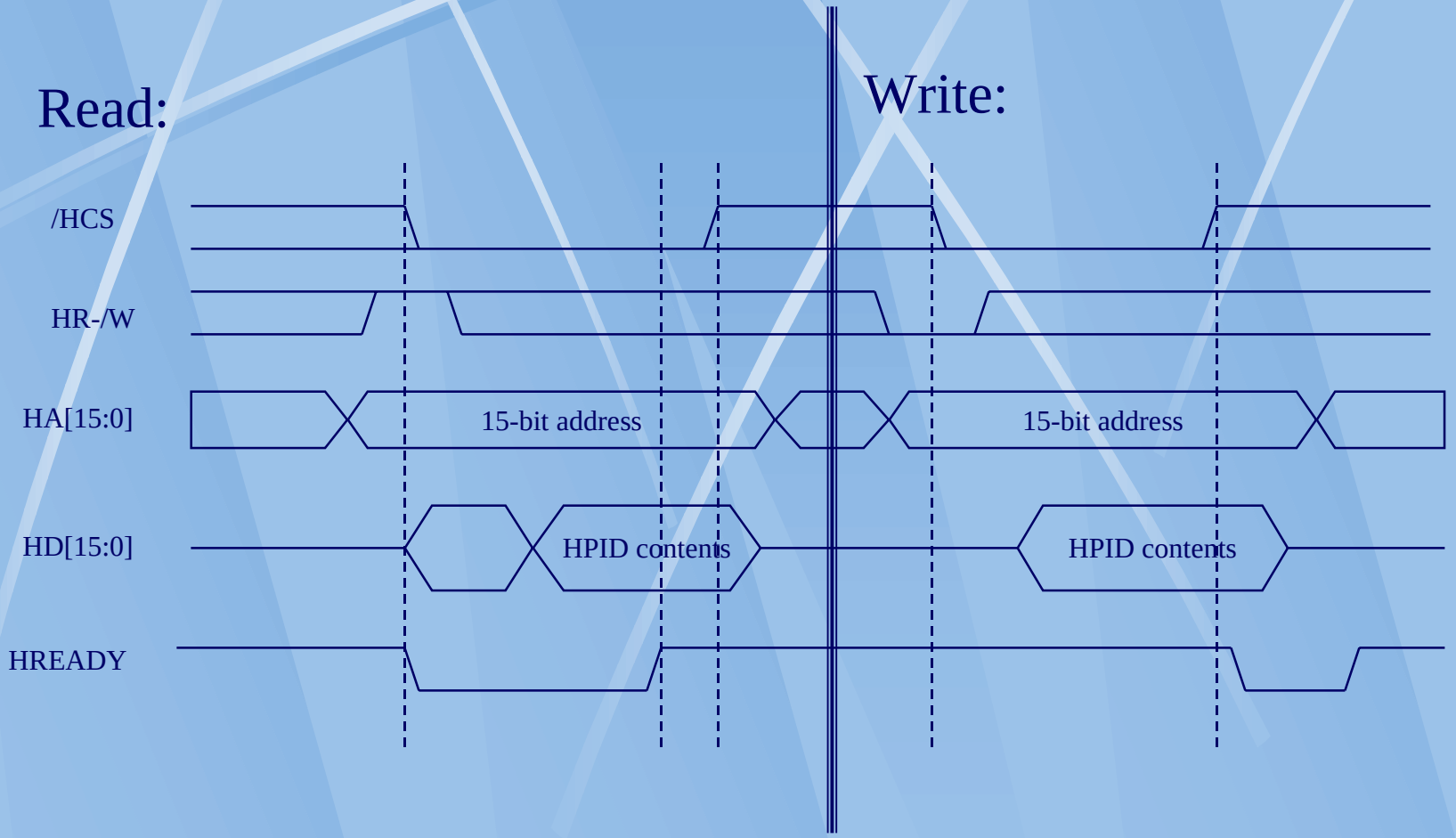
Inter-DSP Communication:

Parallel Bus to HPI Interface Bus



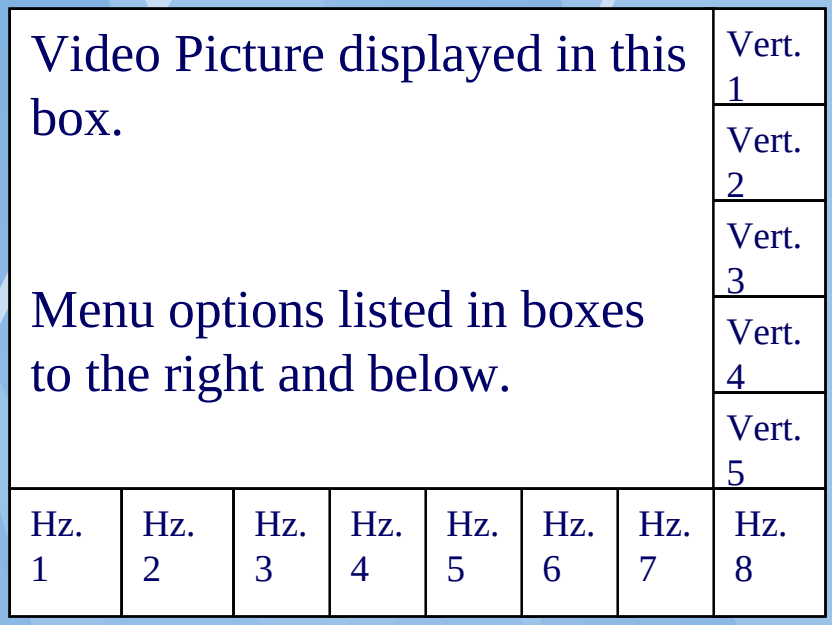
Slave is mapped into master's IO space

HPI Transaction Timing Diagrams:



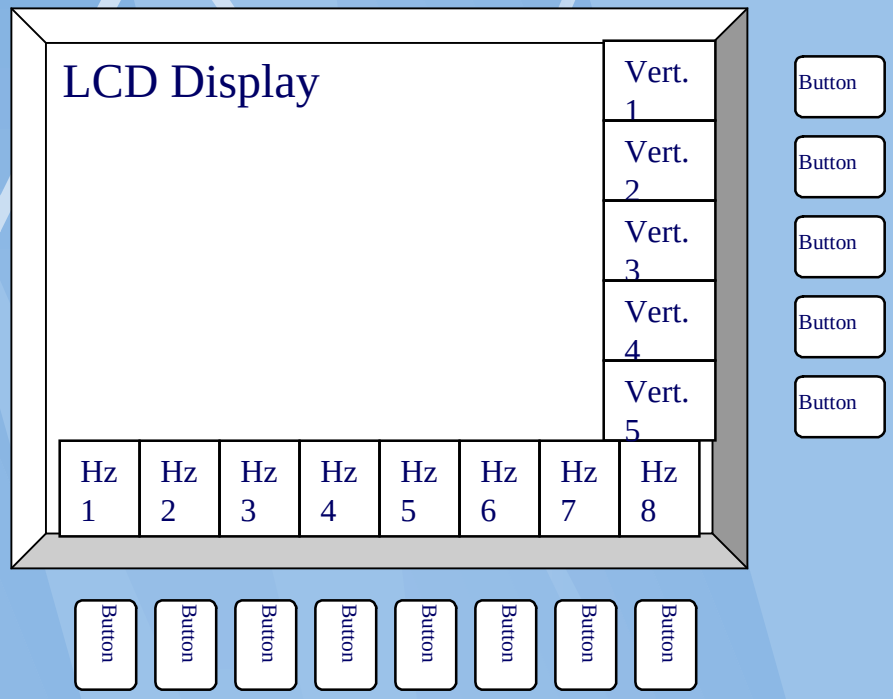
Push-button Interface

- Implements user interface
- Software definable functions
  - Greatly reduces number of physical buttons needed
  - Menu of options displayed on-screen



Push Button Interface

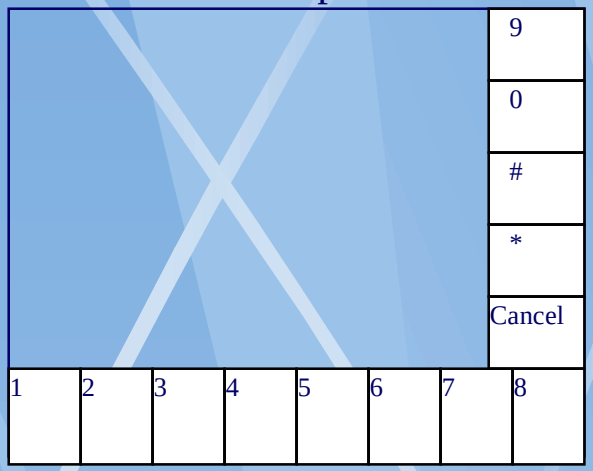
- Physical buttons
  - 13 buttons used
    - Buttons needed for a single function placed together
      - Keeps the interface easy to use
    - Making a call requires 0-9, #, *, and “Cancel”
  - Placed around LCD screen
    - Adjacent to on-screen menu options



Interface Flow Example (1):

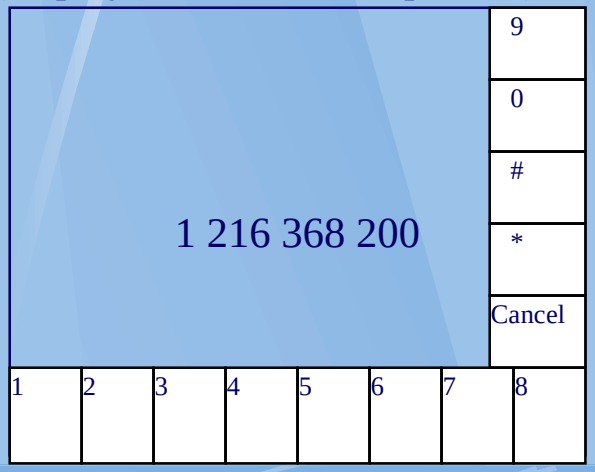
1: Initial Menu:

2: "Place Call" is pressed



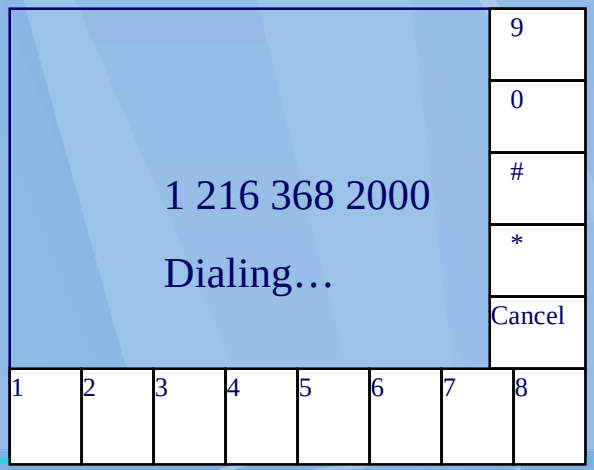
3: Numbers/Symbols pushed

(displayed on-screen as pushed)



4: a) Sequence completed-- dials

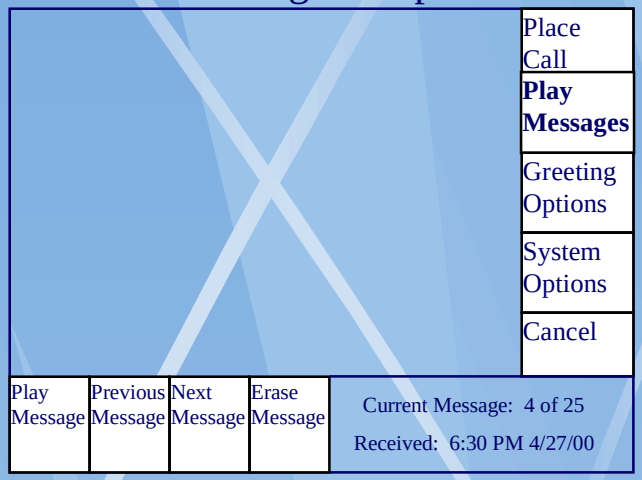
b)"Cancel" pushed – returns (1)



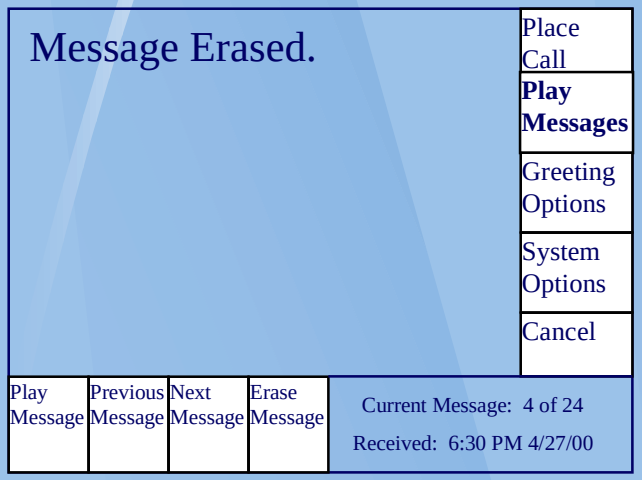
Interface Flow Example (2):

1: Initial Menu:

2: "Place Messages" is pressed



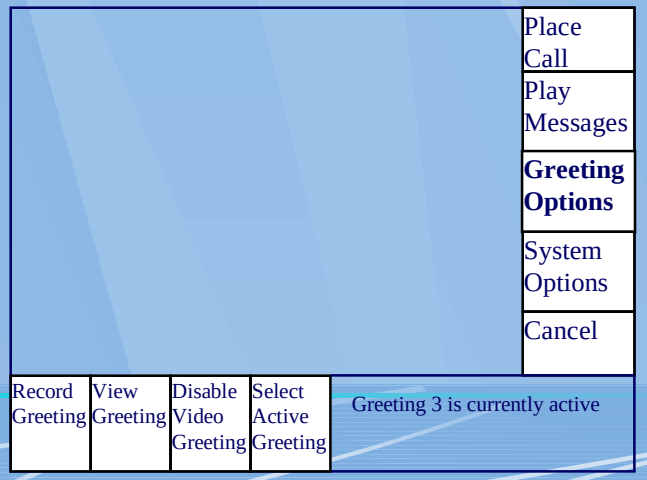
3: a) "Erase Message" pushed



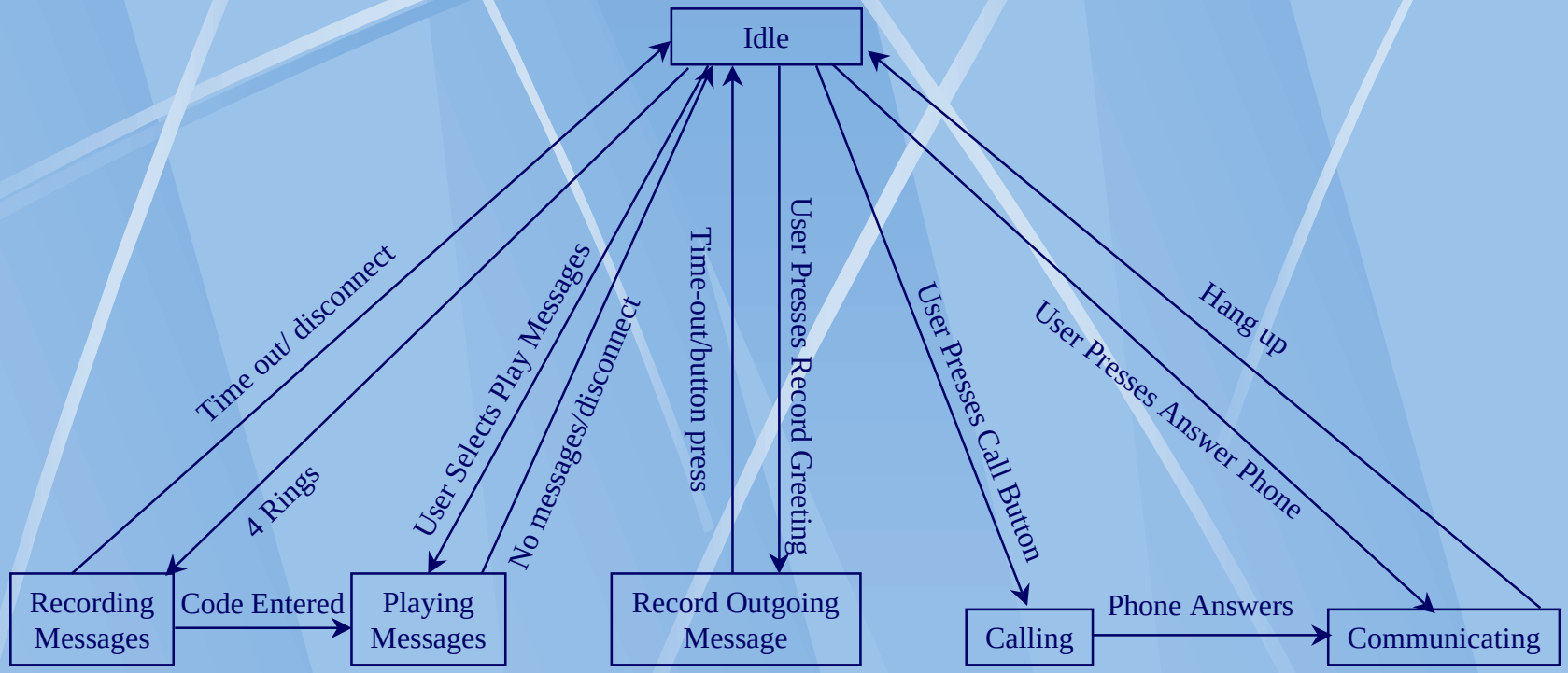
3: b) "Play Message": Plays current message

c) "Cancel" : Returns to 1

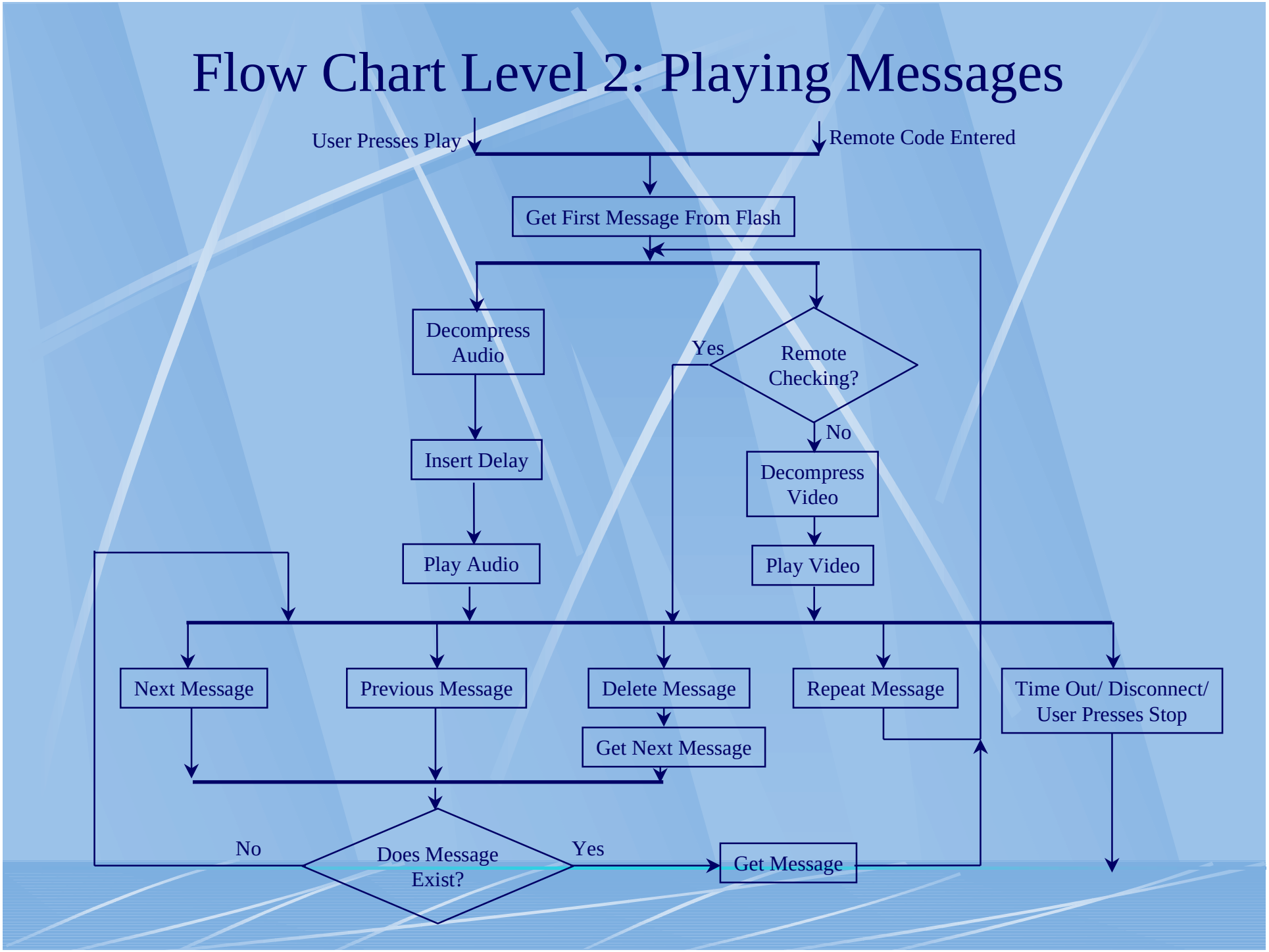
d) "Greeting Options" displays Greeting menu



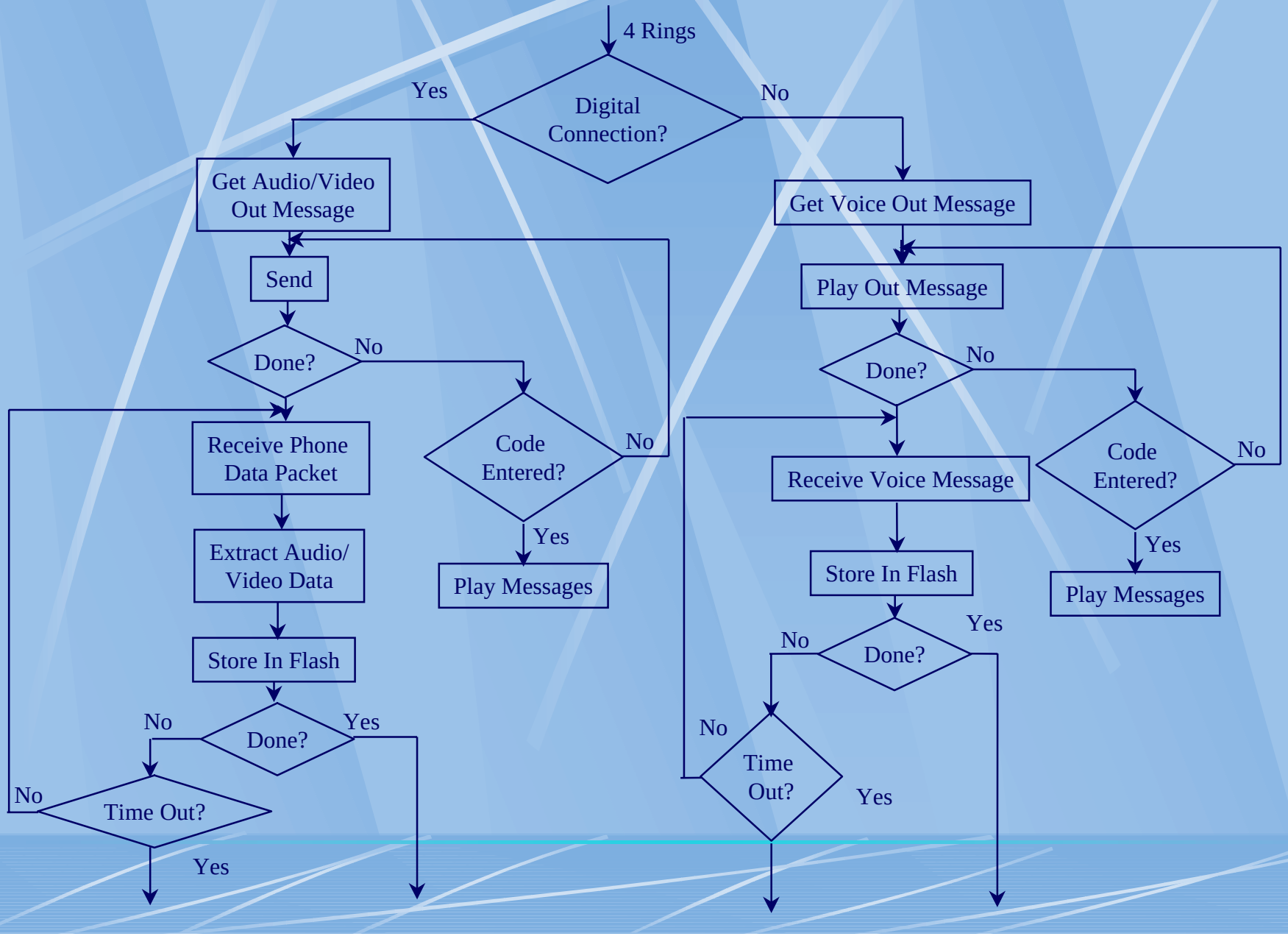
Flow Chart Level 1



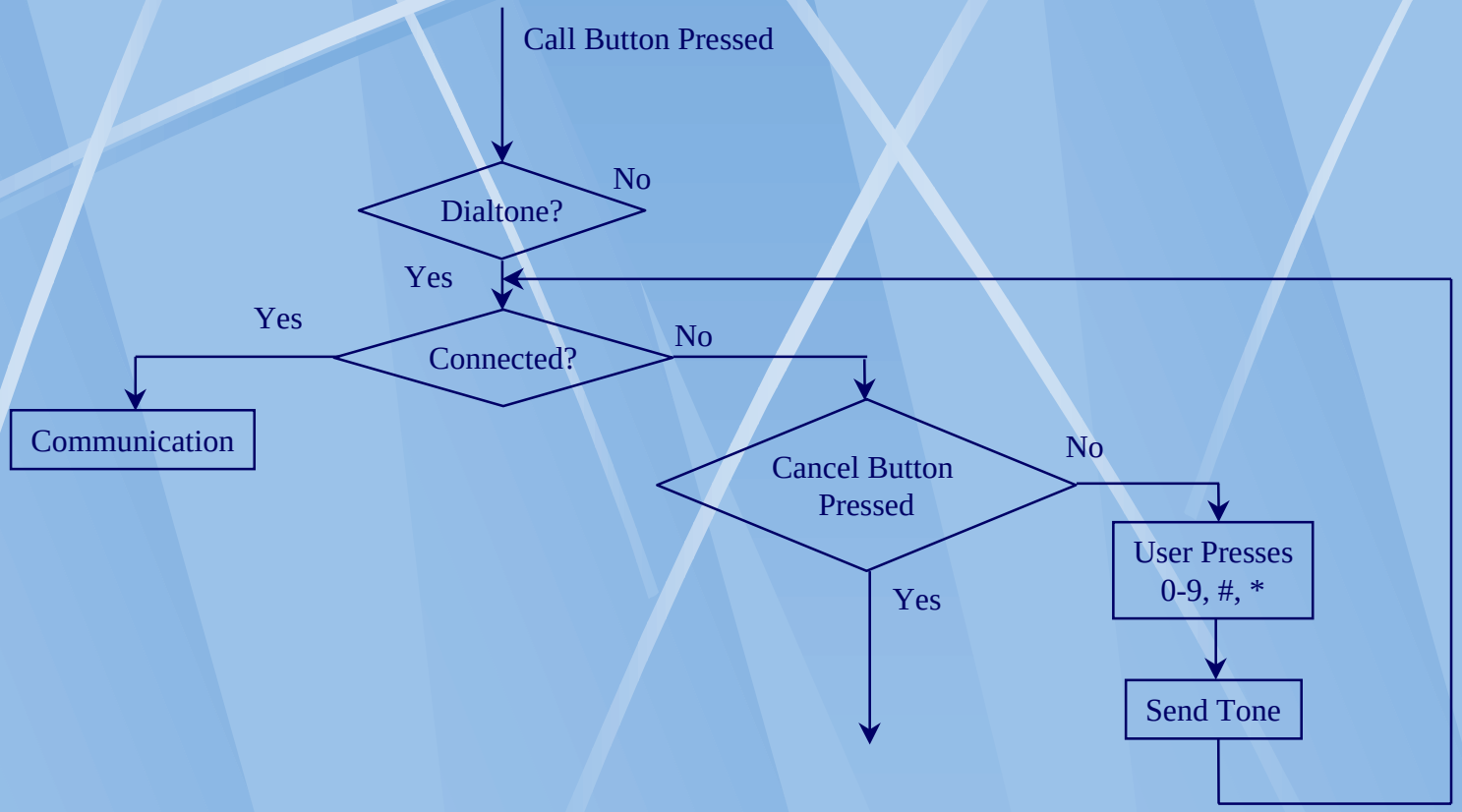
Flow Chart Level 2: Playing Messages



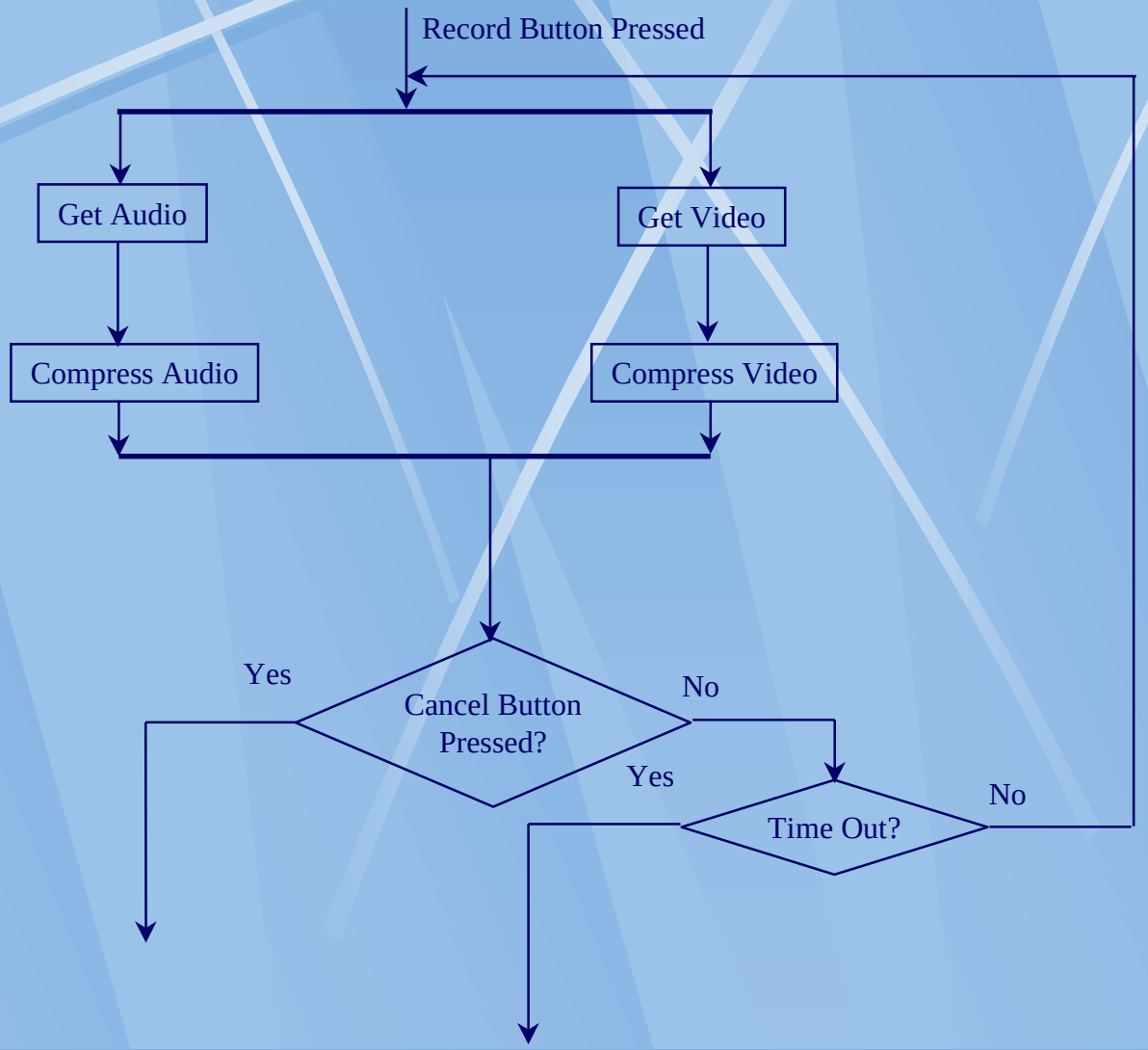
Flow Chart Level 2: Recording Messages



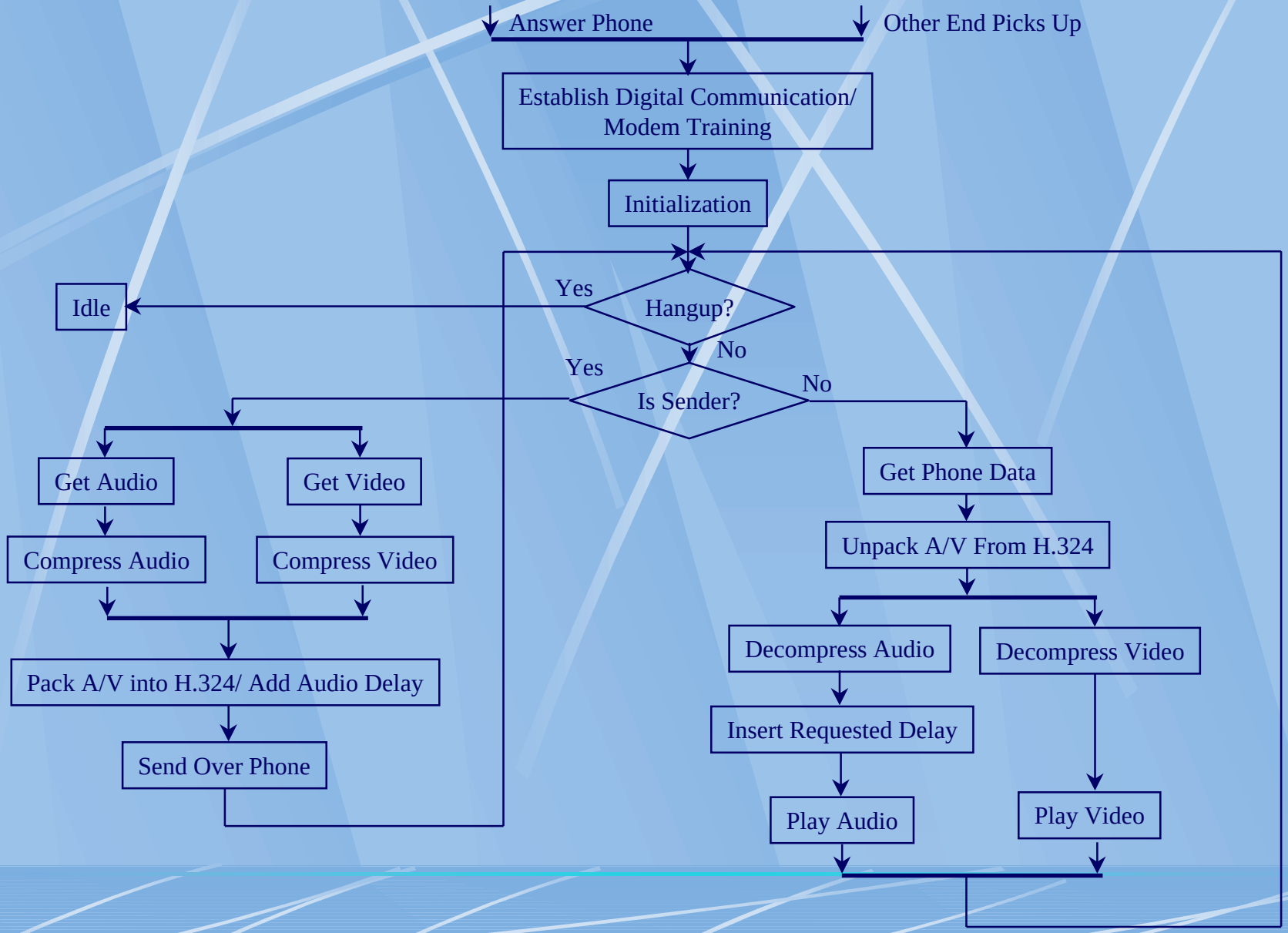
Flow Chart Level 2: Calling



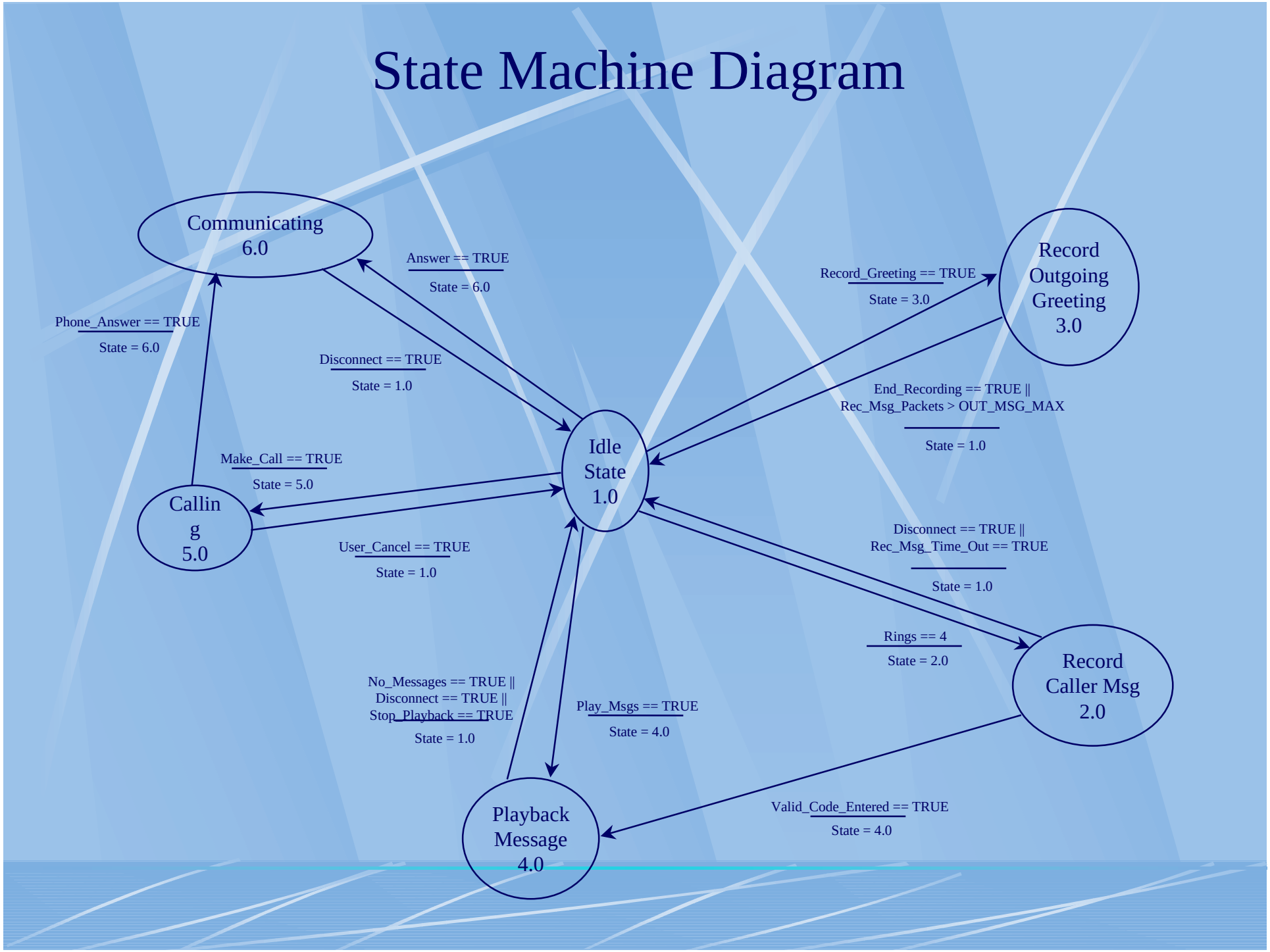
Flow Chart Level 2: Record Outgoing Message



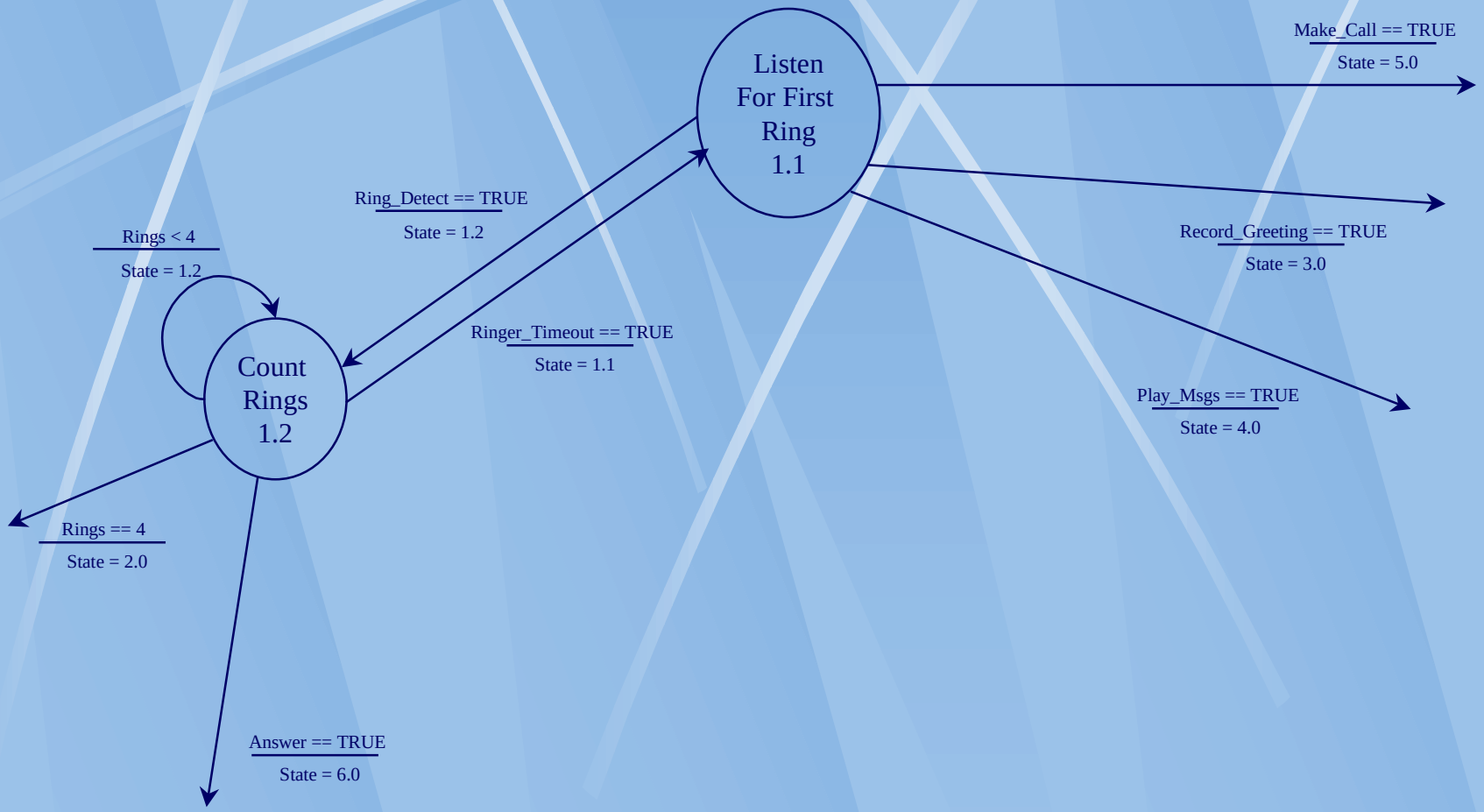
Flow Chart 2: Communication



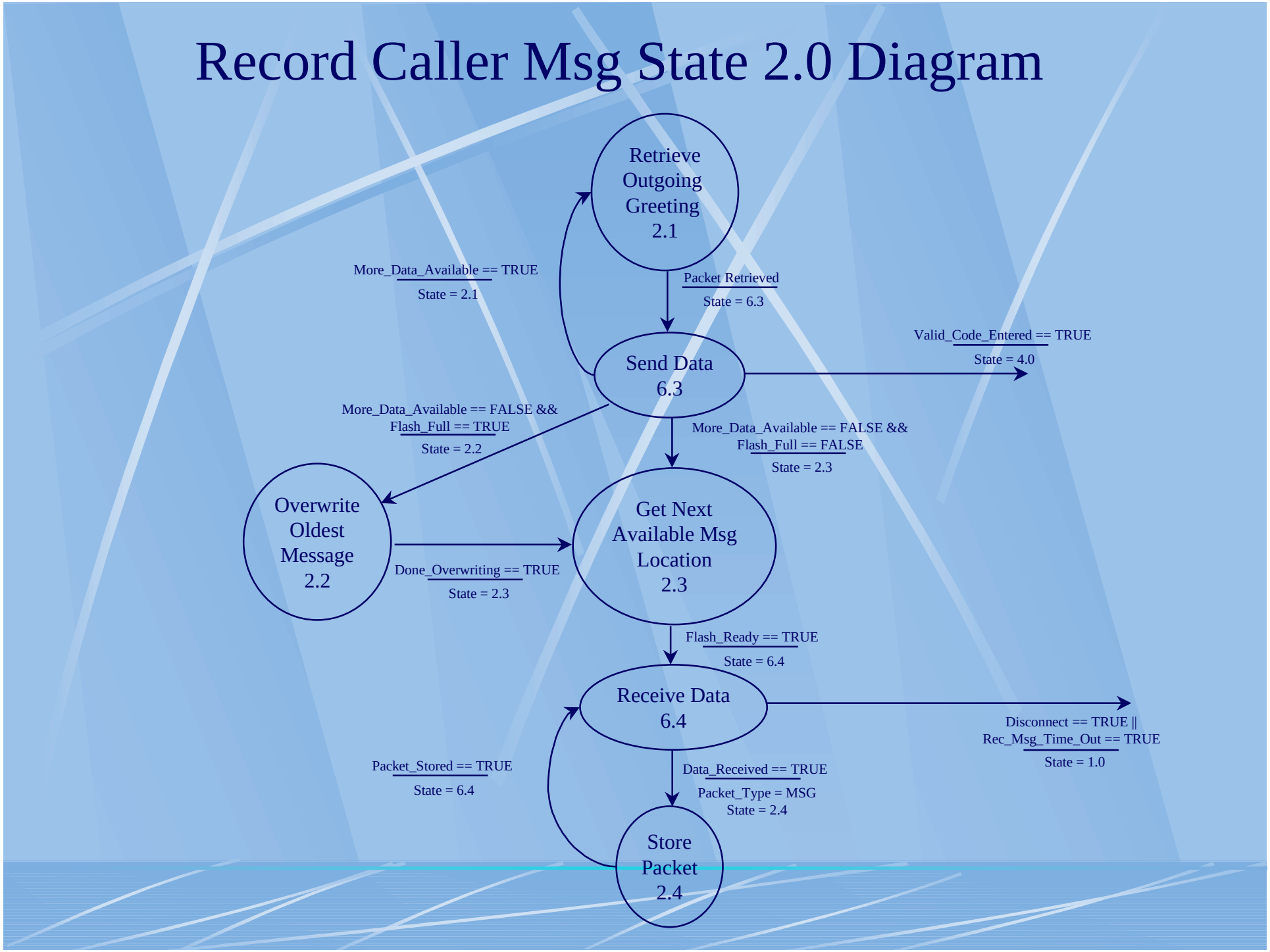
State Machine Diagram



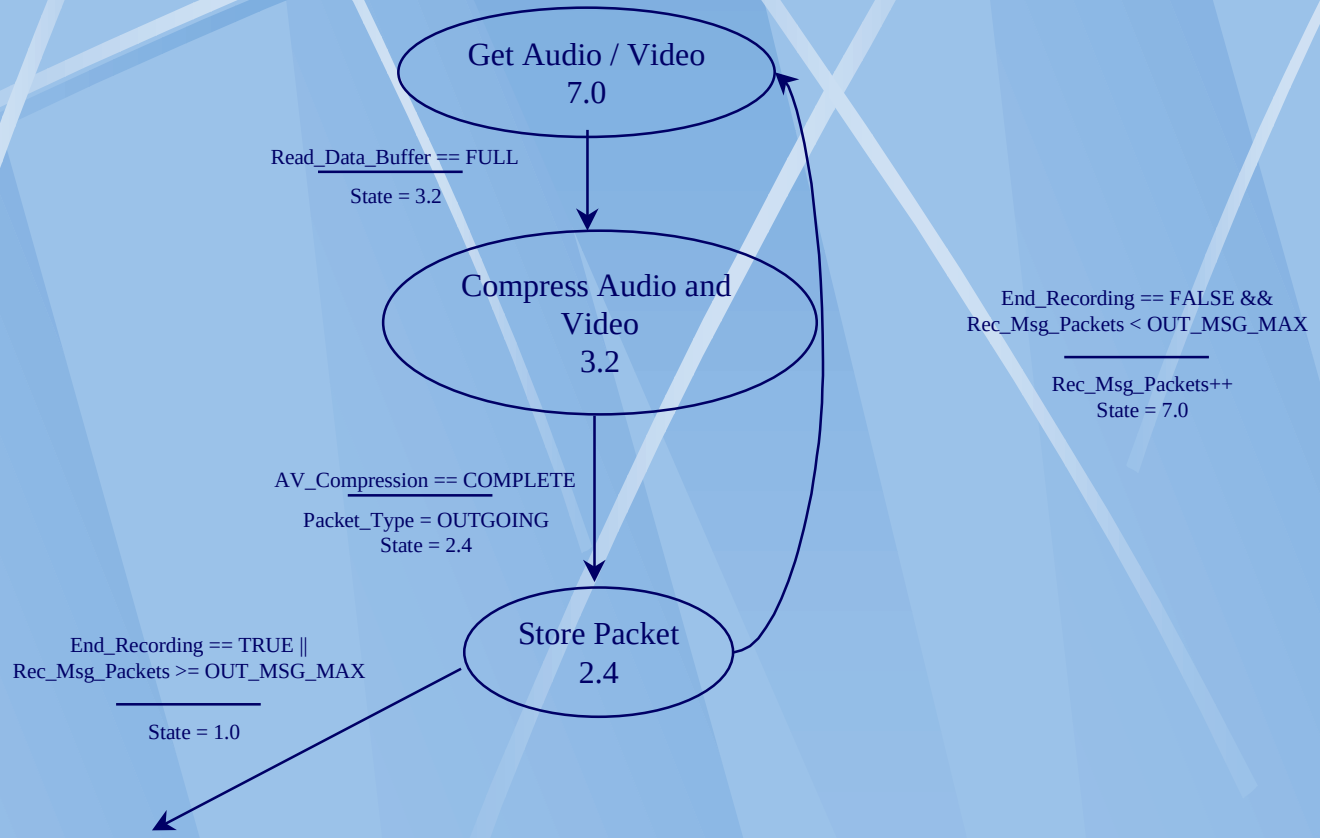
Idle State 1.0 Diagram



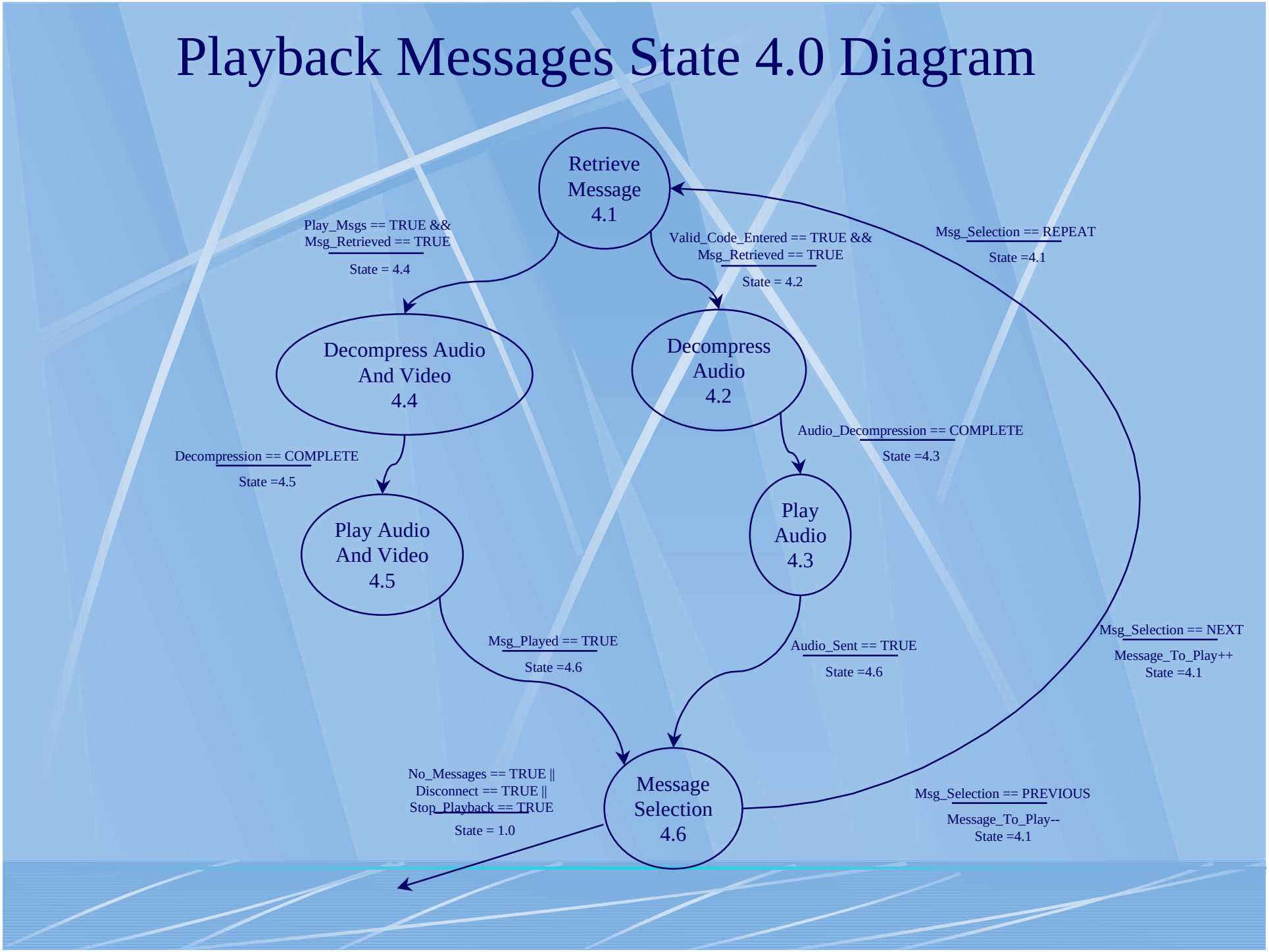
Record Caller Msg State 2.0 Diagram



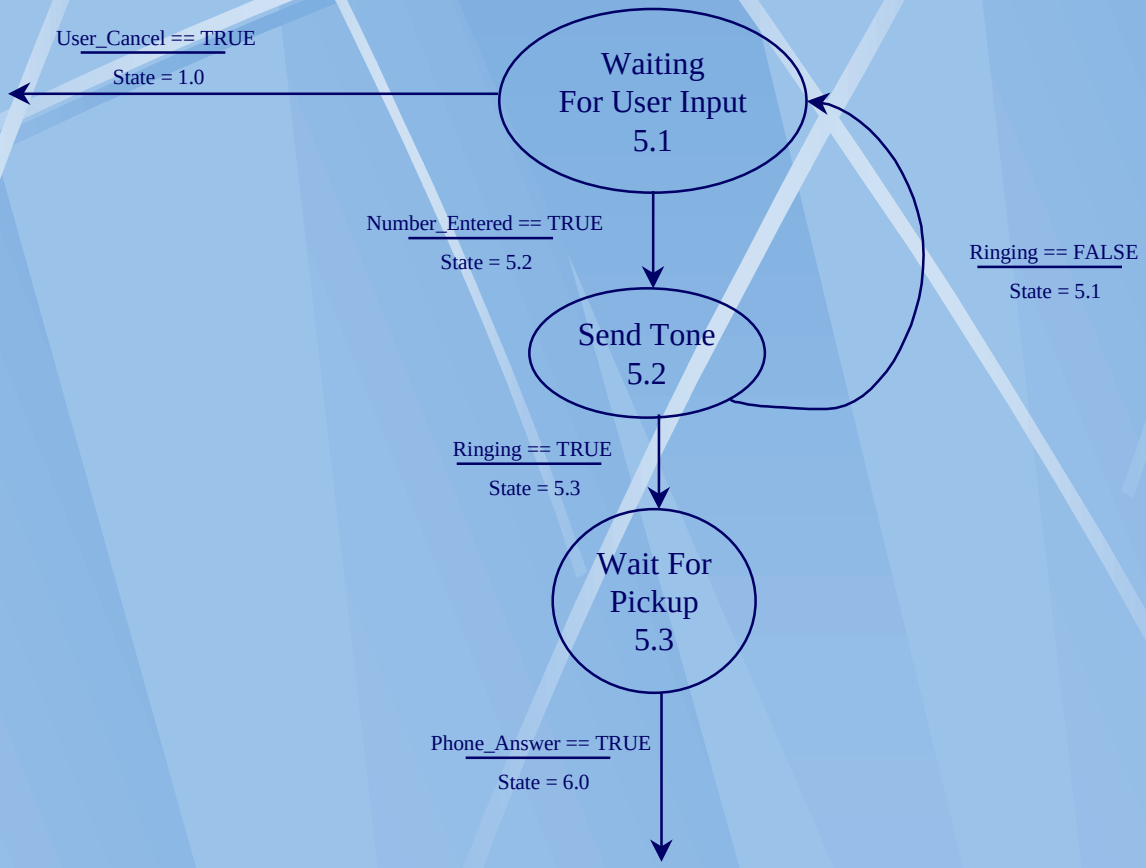
Record Outgoing Greeting State 3.0 Diagram



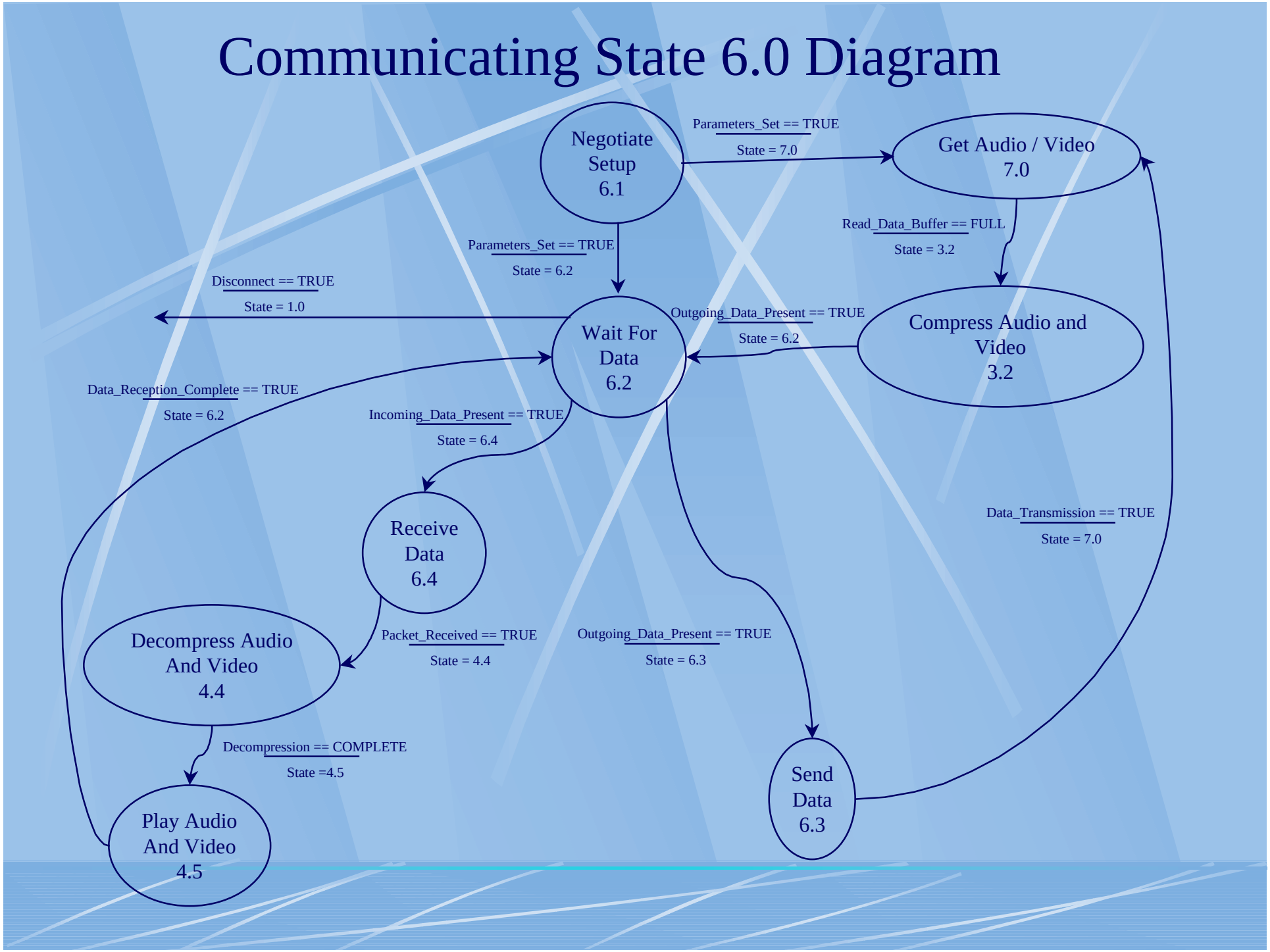
Playback Messages State 4.0 Diagram



Calling State 5.0 Diagram



Communicating State 6.0 Diagram



Caller ID – Physical Layer

Physical Layer

- 8 bit Characters Transmitted Asynchronously
- One Start Bit, Between One and Ten Stop Bits
- 1200 baud FSK Modulated Data

Format

S2 M B7 B6 B5 B4 B3 B2 L S1

S1 – Start Bit
S2 – Stop Bit
M – Most Significant Bit
L – Least Significant Bit
B* - Bit Numbers 2 to 7

Most Significant Octet is Transmitted First

Caller ID – Datalink Layer

Channel Seizure	Mark Signal	Message Type	Message Length	Message Presentation Layer	Checksum
80 – 262 ms	> 45 ms	~ 9.8 ms	~ 9.8 ms	0 – 2488 ms	~ 9.8 ms
96 – 315 bits	> 55 bits	8 bits	8 bits	0 – 2040 bits	8 bits

Channel Seizure – Phasing Pattern of Alternating 1's and 0's

Mark Signal – A Series of Mark Bits (1's)

Message Type – Application Dependent

Checksum – 2's Complement Sum of all Bytes From "Message Type" Word

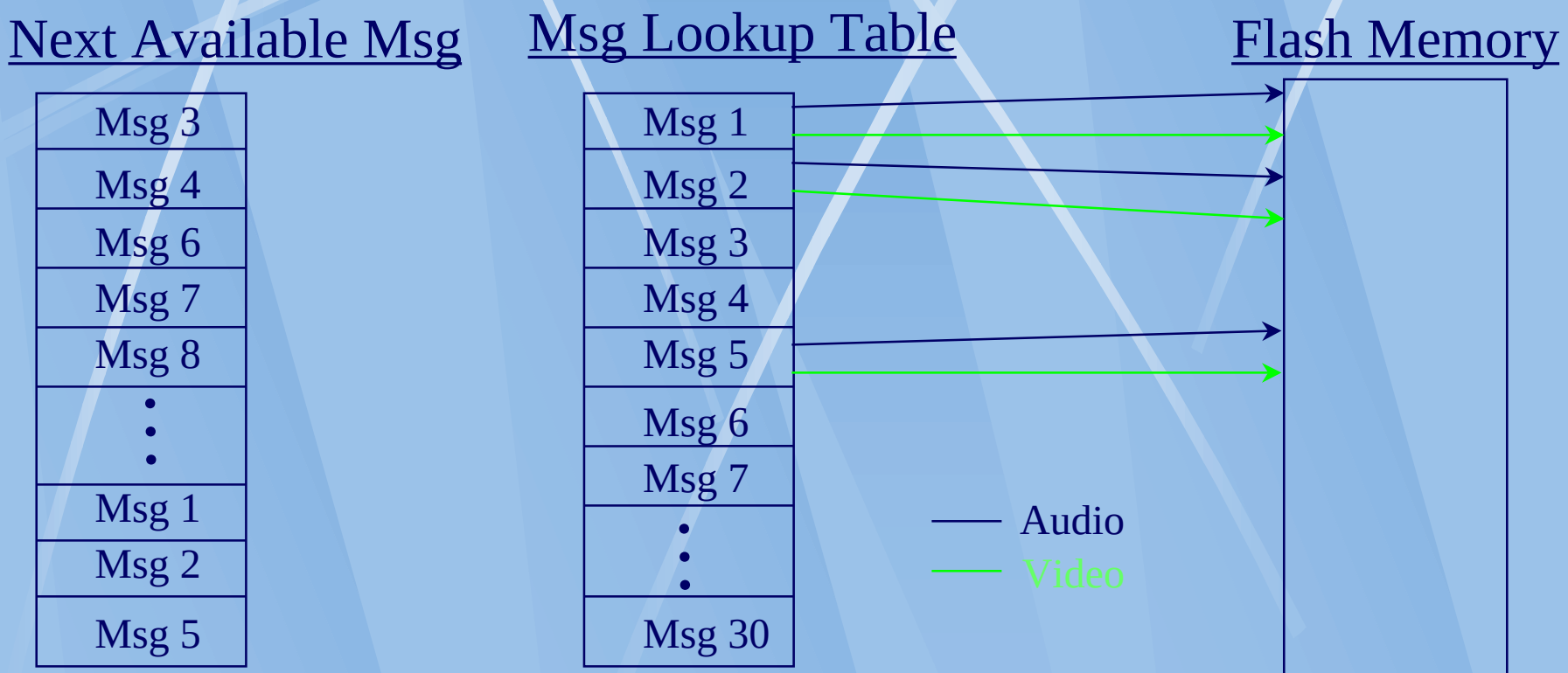
Caller ID – Presentation Layer

Parameter Type	Parameter Length	Parameter Byte(s)	…	Parameter Type	Parameter Length	Parameter Byte(s)

Parameter Type

1 – Time & Date
2 – Calling Line Directory Number (DN)
3 – Called Directory Number
4 – Reason for Absence of DN
7 – Caller Name / Text
8 – Reason for Absence of Name
17 – Call Type
19 – Network Message System Status

Messaging



When a message is recorded, it is put on the bottom of the Next Available Msg buffer

When a message is deleted, it is put on the top of the Next Available Msg buffer

Interphone Communication

- Follow H.245 control protocols
  - Mandated by H.324
  - Overview
    - Master/Slave relationship between terminals
      - Based on terminal type or random #
    - Machines exchange capabilities
      - Master transmits preferences
      - Slave accepts/rejects
        - Based on capabilities and settings
    - Master establishes channels for data transfer
    - Data transferred

Conclusions

- Potential per unit profit margin: $215
  - Low competitor's retail: $450
  - Per unit expense: $235
- Competitively featured
  - H.324 compliant
  - Video messaging capabilities
  - Slick UI
- Solid Design Foundation
  - Ease Implementation Issues
  - Facilitate quick time to market